
# ADDAPT

# Adaptive Data and Power Aware Transceivers for Optical Communications

**Deliverable Report D 5.1**

# Specifications for adaptive transceiver ICs

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## Confirmation

Any work or result described in this report is either genuinely a result of this project or properly referenced.

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## Version Management

**Table 1 List of Revisions**

| Version | Description | Author | Released |
|---|---|---|---|
| **V0** | First setup; template | R. Henker (TUD) | July 24, 2014 |
| **V01** | Input sections 4.2.1, 4.3.1 | J. Pliva, M. Khafaji (TUD) | August 18, 2014 |
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## Executive Summary

This report describes the initial concepts and specifications for the transceiver ICs of the ADDAPT research project. The design includes the main circuits of laserdiode driver (LDD), transimpedance amplifier (TIA), limiting amplifier (LA) and clock- and data-recovery (CDR). These ICs will be designed in 14 nm CMOS technology for high speed with data rates up to 56 Gb/s and lowest power consumption to achieve a high energy efficiency of all together a few pJ/bit. Furthermore, adaptivity with regard to performance (e.g. bandwidth) and power consumption scaling is implemented into the circuits. A rapid switch on/off faster than 20 ns and an adaptive performance tuning for data rates of 56-28-14-7 Gb/s enable the reduction of the power consumption in the optical link. Preliminary simulations revealed that a 50 % energy saving is possible by reducing the bandwidth by 50-70 %. The design of the circuits already started and a first 14 nm CMOS tape-out is expected at the end of 2014. Optionally, 28 nm CMOS might be used for additional circuits to verify basic circuit and adaptivity approaches.

# 1 Introduction

High-speed electrical transceiver circuits are the main system components which are able to react flexibly on varying bitrates of dynamic networks. The optical devices are primary steered by the ICs, thus depending on their adaptivity capabilities. Moreover, electrical ICs usually consume lots of power. Therefore, special focus is given on the power-efficient design and on adaptivity enabled by novel circuit concepts. The IC includes especially the development of laserdiode driver (LDD) plus level and power control circuits, transimpedance amplifier (TIA), limiting amplifier (LA) and clock- and data-recovery (CDR) circuits. If the transceiver is dedicated for standards dealing with sub-data rates optionally multiplexers, demultiplexers and frequency divider circuits are implemented which will be evaluated in the market study and system design phase.

This report, as first deliverable report of WP5, summarizes first concepts and specifications for the design of the transceiver ICs. Different aspects such as market, application and standard demands but also technical feasibilities with regard to the used technologies, the overall system concept and the packaging approaches are taken into account. The main goals for the IC design are to achieve a very high bandwidth to enable data rates up to 56 Gb/s, a very low power consumption for high energy efficiencies in the order of 2 pJ/bit for TX and Rx each, compactness of the circuits to guarantee high parallelization and adaptivity with regard to scalable performance (e.g. bandwidth) and power consumption.

In Section 2 an introduction on the general scope and objectives of WP5 ‘Adaptive ICs’ and a brief description of the task T5.1 ‘Concepts and specifications for integrated circuits’ is given. The fundamental and influencing aspects for the investigation of the concepts and specifications of the ICs are described in Section 3. This includes a short review about the state of the art, the requirements and links to other WPs, information on the used technologies and an overview about the system concept. Based on these fundamentals the concepts and specifications, which have been derived by now, are explained. Besides the introduction of adaptivity concepts, the IC design concepts for the transceiver TX and RX parts are described in Section 4. At the end of the report Section 5 concludes the work on T5.1 and gives a brief outlook on following tasks.

# 2 WP5 – Adaptive integrated circuits

## 2.1 *Scope and objective of IC design*

In WP5 of the ADDAPT project the ICs for the transceiver are designed for a high data rate of up to 56 Gb/s and a low power consumption resulting in high energy efficiency. Among these circuits are LDD, TIA/LA, CDR and additional circuitry which is needed for adaptivity control and for the electrical interface to the application system. Power and performance adaptivity is applied by changing the bias current, the clock frequency and if fruitful the bias voltage. Furthermore, the use of emphasis or equalization techniques and advanced modulation coding schemes are considered to enhance the possible data rate. The design of the electrical transceiver ICs will be realized in very advanced 14 nm IBM CMOS technology and aims adjustable data rates from 7 up to 56 Gb/s. In addition 28 nm CMOS can be used to implement and evaluate different circuit topologies, peaking methods and adaptivity approaches, since the use of the 14 nm technology is strongly limited. However, the concepts can be transferred into the 14 nm technology afterwards. Successful IC design requires the knowledge of exact models of the optical components and their connections to the ICs. Bandwidth peaking techniques such as inductive series peaking, inductive load peaking, transformer coupled peaking and emitter degeneration with parallel RC elements will be considered to further relax the speed-to-power consumption trade-offs.

The general design procedure of the circuits will be as follows: 1) Definition of the specifications, 2) Choice of circuit architecture and circuit design, 3) Simulations based on technology design-kit 4) Layout of fabrication ready file including design rule check, parasitic extractions, etc. 5) Fabrication 6) Measurements, and 7) Redesign and optimization. Three IC design runs in 14 nm CMOS are planed with one approximately every 12 months. In the first iteration step single initial high-speed designs are developed to achieve for the first time 56 Gb/s circuits with lowest power consumption. Simultaneously, these designs are used to verify the models of the optical components and the CMOS technology as well as its process variations. Pre-/deemphasize and equalization technologies will be used to relax the bandwidth requirements of the ICs and the optical components. This first IC run will be used to implement a one lane subsystem which will be used for the verification of the speed, low power consumption and the rapid on/off switching of the link.

On this basis the circuits will be further optimized in the second run and equipped with the adaptive tuning concepts. In the third run the four lane TX and RX system will be integrated on one chip. During fabrication of the 14 nm chips, 28 nm will be used for additional tape-outs of single ICs. Standard computer-aided design-tools such as Cadence and HFSS will be used for the development work. WP5 is coordinated by TUD.

## 2.2 *Task 5.1 – Concepts and specifications for integrated circuits*

Based on the insights gained in WP2 (market analysis) and WP3 (system design), concepts and specifications for the realization of the transceiver ICs are derived in this task. Also the boundaries regarding the optical devices (WP4) and the packaging (WP6) are taken into account. In the

following of this report, the interdependencies of these aspects are explained in more detail and the initial IC concepts and specifications are described.

# 3 Fundamentals

## 3.1 *State-of-the-art*

In this section a brief review of the state of the art on the main ICs of the ADDAPT transceiver is given which shows that new implementations and concepts are required to achieve the data rate, power consumption and adaptivity targets. The participating partners in ADDAPT (IBM and TUD) already have been active in the design of those ICs and thus can build on a deep knowledge in these fields.

The state-of-the-art of high-speed laser drivers (LDD) is listed in Table 2. Bit rates up to 40 Gb/s or higher without pre-emphasis were achieved only in BiCMOS. In 90 nm and 0.13 µm CMOS, speeds up to 20 Gb/s were reported. No speed and power adaptivity issues were considered in these works. Only one work was found where the power consumption can be reduced at lower bandwidth. This is enabled by tuning the supply voltage. No tuning of the IC's supply and laser modulation current was considered for this IC which yields a maximum data rate of only 8 Gb/s. LDDs with pre-emphasis show data rates of 40 Gb/s as well and above. The power consumption of those circuits is very high and therefore the energy per bit is with >3 pJ/bit very high as well. One reason for this might be the use of a BiCMOS technology which is usually more power hungry than CMOS technologies. Thus, in ADDAPT it will be investigated how the power consumption of a LDD with pre-emphasis/equalization techniques can be lowered using highly scaled 14nm CMOS technology.

**Table 2 Comparison of state-of-the-art high-speed laser drivers**

| Speed/power adaptivity | Bitrate | Supply power | Energy efficiency | Pre-emphasis/ equalization | Technology | Ref. |
|---|---|---|---|---|---|---|
| No | 12.5 Gb/s | 27 mW | 2.16 pJ/bit | No | 90 nm CMOS | [1] |
| No | 40 Gb/s | 80 mW | 2 pJ/bit | No | 0.18 µm BiCMOS | [2] |
| No | 18 Gb/s | 14 mW | 0.8 pJ/bit | No | 90 nm CMOS | [3] |
| Yes - supply voltage | 4-8 Gb/s, scalable | 9-27 mW, scalable | 2.25-3.4 pJ/bit | No | 0.13 µm CMOS | [4] |
| No | 40 Gb/s | 130 mW | 3.25 pJ/bit | Yes | 0.25 µm BiCMOS | [5] |
| No | 64 Gb/s | 900 mW | 14 pJ/bit | Yes | 0.13 µm BiCMOS | [6] |
| No | 40 Gb/s | 312 mW | 7.8 pJ/bit | yes | 0.13 µm BiCMOS | [7] |

In Table 3, the state-of-the-art parameters of high-speed transimpedance amplifiers (TIAs) ia shown. 40 to 50 Gb/s TIAs in BiCMOS, as well as in 45, 65 and 90 nm CMOS, were demonstrated.

The list includes also 4 designs published by TUD. The circuits mainly use common source or cascade circuits with feedback and common gate stages. Most of these designs do not consider any adaptivity and are optimized for fixed DC bias points. The only circuit addressing speed and power issues provides a tuning from 4 to 8 Gb/s and correspondingly a reduction of the supply power was shown by tuning the supply voltage.

**Table 3 Comparison of state-of-the-art high-speed TIAs**

| Speed/ power adaptivity | Data rate | Transim-pedance gain | Power con-sumption | Energy efficiency | PD capacitance | Noise current | Techn. | Ref. |
|---|---|---|---|---|---|---|---|---|
| No | 10 Gb/s | 57 dBΩ | 1.8 mW | 0.18 pJ/bit | 200 fF | 30 pA/√Hz | 0.13 µm CMOS | [8] |
| No | 10 Gb/s | 80 dBΩ | 6 mW | 0.6 pJ/bit | 330 fF | 32 pA/√Hz | 80 nm CMOS | [9] |
| No | 12 Gb/s | 48 dBΩ | 14 mW | 1.17 pJ/bit | 330 fF | n.a. | 90 nm CMOS | [3] |
| No | 28 Gb/s | 76 dBΩ | 29 mW | 1.04 pJ/bit | 100 fF | n.a. | 28 nm CMOS | [10] |
| No | 40 Gb/s | 45 dBΩ | 8.2 mW | 0.2 pJ/bit | 200 fF | 30 pA/√Hz | 65 nm CMOS | [11] |
| No | 40 Gb/s | 75.5 dBΩ | 150 mW | 3.75 pJ/bit | >100 fF | 25 pA/√Hz | 0.25 µm BiCMOS | [12] |
| No | 40 Gb/s | 73 dBΩ | 32 mW | 0.8 pJ/bit | n.a. | 16 pA/√Hz | 0.25 µm BiCMOS | [13] |
| No | 40 Gb/s | 55 dBΩ | 9 mW | 0.3 pJ/bit | 30-80 fF | 20.5 pA/√Hz | 45 nm CMOS | [14] |
| No | 50 Gb/s | 54 dBΩ | 14 mW | 0.28 pJ/bit | 100 fF | 11 pA/√Hz | 0.13 µm BiCMOS | [15] |
| Yes-voltage | 4-8 Gb/s | 56-59 dBΩ | 0.5-2.2 mW | 0.13-0.28 pJ/bit | n.a | n.a. | 0.13 µm CMOS | [4] |

Clock data recovery (CDR) circuits are basically difficult to compare in its parameters since they can differ much due to the design, optimization and requirements according to different applications. However, referring to Table 4, high-speed CMOS CDRs reach data rates of 40 Gb/s at a supply power below 100 mW. These circuits were designed in 90 and 65 nm CMOS. Some of these circuits allow an adjustment of the speed. However, no scaling of the power consumption is considered and no information could be found in literature about scaling of the power consumption in CDRs at low data rates.

**Table 4 State of the art CDRs**

| Speed/power adaptivity | Data rate [Gb/s] | Supply power [mW] | Energy Efficiency [pJ/bit] | CMOS [nm] | Ref. |
|---|---|---|---|---|---|
| No | 40 | 144 | 3.6 | 180 | [16] |
| No | 40 | 48 | 1.2 | 90 | [17] |
| No | 25 | 172 | 6.9 | 90 | [18] |
| No | 40-44, scalable | 900 | 20.5 | 90 | [19] |
| No | 6-44, scalable | 230 | 38-5.2 | 90 | [20] |
| No | 27-40, scalable | 72 | 2.7-1.8 | 65 | [21] |

As can be seen from this review no energy efficient implementations for 56 Gb/s are available or have been presented so far. Furthermore, a scaling of the bandwidth and the power consumption has been shown in one case only, but for much smaller data rates. For some circuits the energy efficiency is very high. By going to even higher data rates, this will further increase. It has to be evaluated how much the power consumption of such ICs can be lowered by using the 14 nm CMOS technology.

## 3.2 *Interdependencies, requirements and link to further aspects of other WPs*

For the development of the IC concepts and specifications different aspect are considered. From the market, application and standardization studies in WP2 it has been figured out that in the near future single channel data rates of more than 50 Gb/s are required. For example in Infiniband the HDR and NDR requests 50 Gb/s and 100 Gb/s, respectively. For Ethernet it is expected that that the servers have to provide 100-Gigabit Ethernet in 2017. More details about potential applications and markets for the ADDAPT approaches are given in deliverable report D2.2 which has been presented in April 2014. Therefore, an increase of the transceiver channel data rates is mandatory and for the ADDAPT ICs a data rate of up to 56 Gb/s is targeted. At the same time, the aim of network, data center and high performance computing operators is to lower the power consumption of the systems in order to save energy, lower the heat dissipation and therefore the cooling efforts and last but not least to reduce the operating costs significantly. Thus, the power consumption of the ICs have to be lowered which can be achieved by using advanced and highly scaled low power technologies like 14 nm CMOS leading to high energy efficiency. Furthermore, the optical links with static performance of today have to become variable and dynamic in future with regard to changing demands and conditions in the network. Performance and power adaptivity in the links enabled by adaptive circuits will be one solution to achieve an additional energy saving. This needs to equip the ICs with capabilities for a rapid on/off switching and tuning of their bandwidth and power consumption.

From the technical point of view the design of the ICs is strongly connected to other technical aspects of other WPs such as the system concept, optical components and the assembling and

packaging. From initial studies on the optical components it has been figured out that for the vertical-cavity surface-emitting lasers (VCSEL) it will be difficult to achieve a data rate of 56 Gb/s by themselves due to physical limits. Thus, the LDD has to provide a proper pre-emphasis or equalization technique to overcome the bandwidth bottleneck of the VCSELs. Furthermore, the LDD has to provide sufficient bias as well as modulation voltages and currents to the laser. On RX side the TIA has to deal with very weak photocurrents due to low optical received powers. Thus, the TIA should have a high sensitivity, while the amplification should be high and the noise should be minimal. Regarding assembling and packaging the ICs are required to enable wirebond connections which have to be taken into account for pad sizes, positions and pitches. Especially, the pad sizes will have a significant impact on the performance of the ICs due to parasitic capacities. The bondwire connection has to be considered and involved into the IC design as well due to parasitic inductances. From the system concept there will be an array of ICs for four channels necessary. Thus, during the design possible cross talk between the parallel chips has to be carefully considered. The concepts and specification of the optical components and the packaging and assembling techniques, which have influence on the IC design, are explained in more detail in the deliverable reports D4.1 and D6.1 which are already available. A report D3.1 on the details of the system concept and architecture will be available by October 2014.
At least all these aspects were taken into account for the initial concepts and specification of the ICs which are described in the sections below.

## 3.3 *Technology*

For the IC design an advanced 14 nm Thin-FET SOI CMOS technology of IBM is used. This technology combines advantageous properties like high performance, low voltage/energy consumption and highly scaled devices for ultra-compact designs. This is the primarily used technology to realize the electrical transceiver components within ADDAPT.
In addition, a bulk 28 nm CMOS technology of Globalfoundries will be used for implementing and evaluating different approaches for the adaptive operation of the circuits and the control of the performance and power consumption. The performance of this technology might be worse than the performance of the 14 nm technology. However, the basic approaches can be studied and transferred later to the mainly used technology.

## 3.4 *System concept*

The main goal of the transceiver ICs is to demonstrate 56 Gb/s operation with low energy while featuring rapid power on/off functionality. Hence, a prototype circuit including one link path will be manufactured to accommodate the performance targets defined by ADDAPT.
Figure 1 displays the high level block diagram of the test chip including one link path. The test circuit also contains digital blocks to adjust all TX/RX parameters and assist during measurements.
Data to be transmitted are generated on chip and fed to the TX slice. The received photocurrent is converted into voltage by the analog front end (AFE) which consists of TIA followed by LA. Then, the CDR recovers the binary stream. The power up/down sequence on both TX/RX is synchronized

by an external trigger which emulates idle detection, owing to the assumption that in a multi-channel design a master lane will generate the wake-up signal to turn on the slave TX/RX macros.

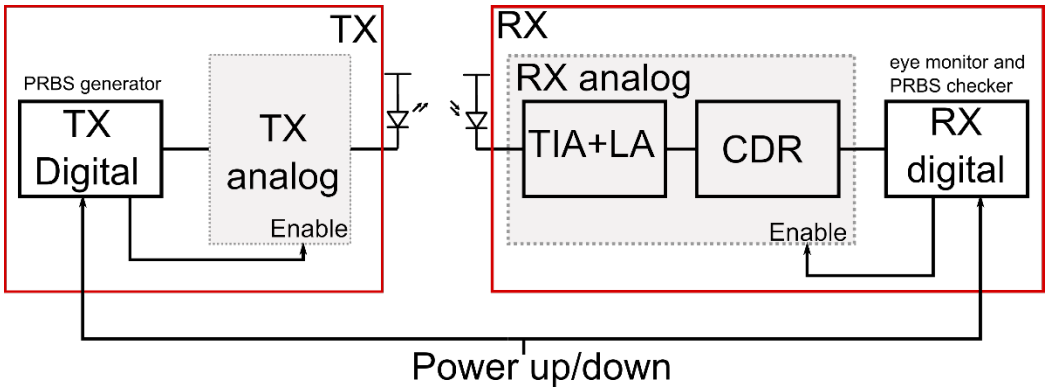



**Figure 1: High level block diagram of adaptive optical link path outlining digitally assisted TX/RX analog macro.**

# 4 IC concepts and specifications

## 4.1 *Adaptive concepts*

To enable power and performance adaptivity according to the actual link data load, rapid on/off switching with switching times <20 ns and bandwidth tuning functionalities are required. To realize the tuning of the circuit's data rates in steps of 56-28-14-7 Gb/s the following concepts are implemented and investigated.

**(a) Transimpedance amplifier**: In Figure 2 the adaptive tuning of a TIA is shown. If lower data rates are sufficient, the supply current $I_{SS}$ can be reduced. At the same time, the bandwidth (BW), which is mainly given by 1/(amplifier input impedance $R_i$ · photodiode capacitance $C_D$) decreases since $R_i \approx R_F/(1+g_mR_D)$, $g_m$ and $f_t$ falls with $I_{SS}$. As a side benefit this decreases the noise which is proportional to BW and $g_m$. If there is any decrease of the effective transimpedance gain $r_T \approx R_F$, this may be compensated by increasing $R_F$ leading to a further acceptable BW reduction. Multi-stage architectures are applied to optimizing bandwidth, transimpedance gain, noise and supply power simultaneously.

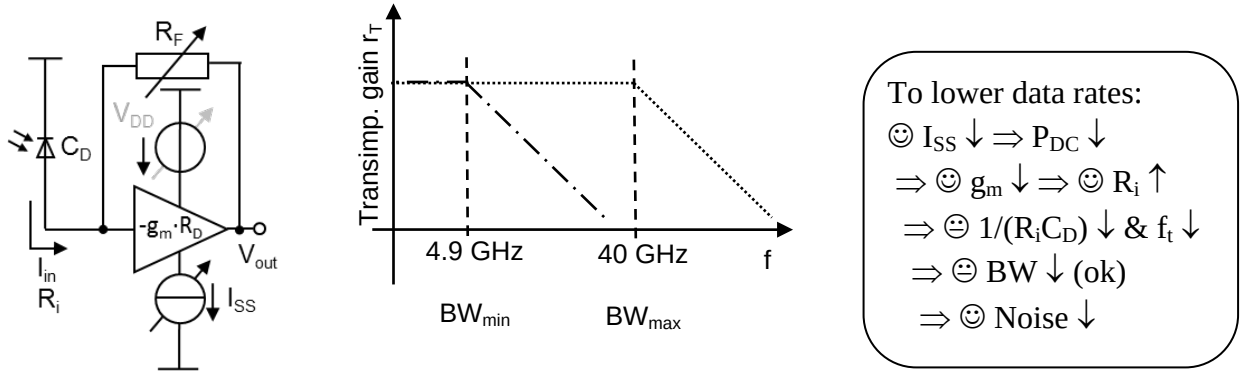



**Figure 2: Adaptive tuning of a TIA; (left) concept, (middle) frequency response, (right) functional chain.**

**(b) Voltage and limiting amplifiers**: In Figure 3 the adaptive tuning of a voltage amplifier or LA is shown. By reducing the current, $g_m$ and consequently the bandwidth BW ~ $1+g_mR_s/2$ decrease. Due to the negative feedback loop, the gain does not change much as long as $g_mR_s/2 >> 1$. If required, the gain and other parameters may be tuned by adjusting also $R_S$ or $R_D$.

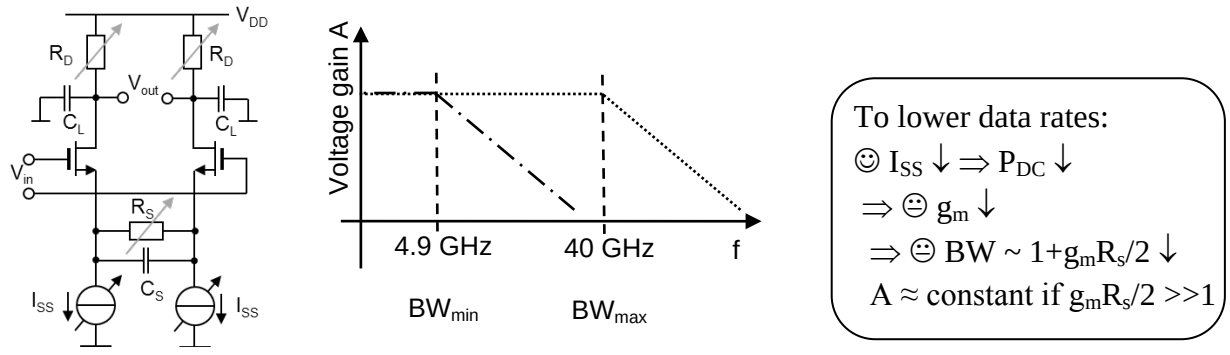



**Figure 3: Adaptive tuning of a LA; (left) concept, (middle) frequency response, (right) functional chain.**

**(c) Laserdiode driver**: Similar power reducing control methods are applied considering also the laser modulation currents and voltages. Circuits like laser drivers typically require a constant output potential versus tuned supply current. This can be done by tuning the load resistance $R_D$ in the driver stages at the same time.

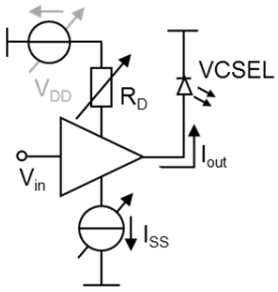
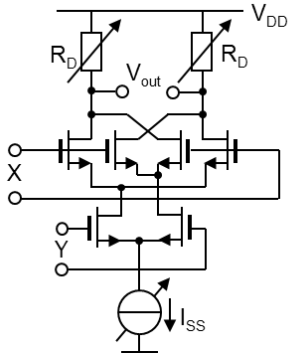



**Figure 4: Adaptive tuning of a LDD.**

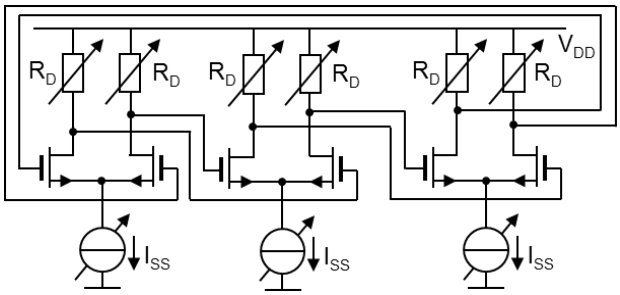
**(d) XOR gate** circuits are required for the CDR circuit, phase detectors and further mixed signal blocks. Also here, similar to the circuits mentioned above, the speed to power consumption ratio can be optimized by tuning the tail currents and the resistive loads. The same optimization can also be achieved for latch circuits and other related circuit designs.




To lower data rates
☺ $I_{SS}\downarrow \Rightarrow P_{DC}\downarrow$
$\Rightarrow$ 😐 $g_m\downarrow \Rightarrow f_t\downarrow \Rightarrow BW\downarrow$
$\Rightarrow$ ☺ noise $\downarrow$
$\Rightarrow$ 😐 $A \approx g_m R_D\downarrow \Rightarrow$ ☺ $R_D\uparrow$ ($\Rightarrow BW\downarrow$)
$\Rightarrow$ ☺ A at reasonable level

**Figure 5: Adaptive tuning of a XOR gate; (left) schematic, (right) functional chain.**

**(e) Oscillators** benefit as well by the proposed techniques. DC current and power can be saved if the clock frequency $f_{ck}$ can be decreased.




To lower data rates:
☺ $I_{SS}\downarrow \Rightarrow f_{ck}\downarrow$
$\Rightarrow$ 😐 gm $\downarrow$
$\Rightarrow$ 😐 $R_D\uparrow \Rightarrow A \sim g_m R_D$ & $V_{out}$ constant
$\Rightarrow$ ☺ $f_{ck}\downarrow \sim 1/(R_D C)$

**Figure 6: Adaptive tuning of an oscillator; (left) schematic, (right) functional chain.**

Preliminary simulations on basic TIA and LDD structures (in a BiCMOS technology) have been performed to evaluate the potential of the current tuning for the scaling of the bandwidth and power consumption. The simulation results are shown in Figure 7. From the diagrams it can be revealed that the power consumption reduces significantly when the bandwidth of the circuits is decreased by scaling down the supply current while the gain remains constant. By reducing the bandwidth to 30-50 % of the peak bandwidth, the power consumption can be reduced by at least 50 %.

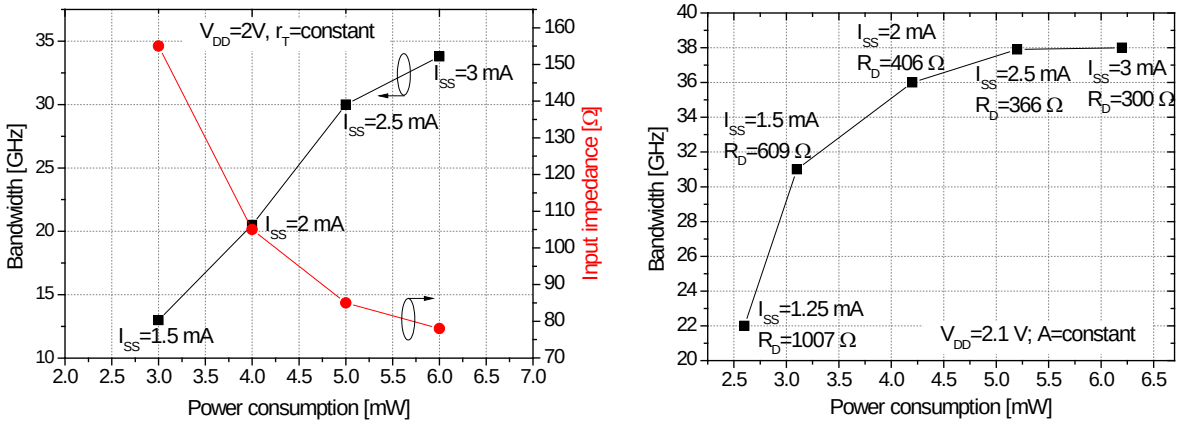



**Figure 7: Simulation of adaptive tuning for (left) TIA and (right) LDD.**

## 4.2 *Transmitter ICs*

### 4.2.1 Laserdiode driver

In this section the challenges of VCSEL driver design are explained. A block diagram of the LDD is shown in Figure 8. One target of the project is to reach a very high bit rate of 56 Gb/s with on-off keying modulation for short range communications. On the other hand, the bandwidth of the VCSELs is around 20 GHz and so driving them at speeds three times higher than their bandwidth necessitates equalization. In literature there are only countable designs reported to date with such rates where the details are not shown [6]. Another big challenge in this regard is that there is no VCSEL model based on measurements which can be directly used during transistor-level circuit design phase or system-level equalizer design. The aforementioned issues enforce us to build a generic VCSEL model which can be used in circuit simulators and also to consider the ability to tune as many parameters as possible in the final hardware to accommodate the characteristics of the VCSEL. This, in turn, is translated to additional complexity of the design and measurement of the driver circuit. Table 5 summarizes the supported range of VCSEL parameters.

**Table 5: Summary of supported VCSEL parameters.**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| **Threshold current** | 0.3 | 1.5 | mA |
| **Slope efficiency** | 0.4 | 0.8 | W/A |
| **Threshold voltage** | 1.5 | 2 | V |
| **Modulation current** | 4 | 8 | mA |
| **Capacitance** | 50 | 350 | fF |
| **Differential resistance** | 50 | 100 | Ω |

Another challenge which has to be considered is the low power design and at the same time tuning the driver power versus link speed. The supply voltage of recent submicron technologies is below 1 V. Therefore all the digital sections, the pre-driver, and equalizer would use this supply voltage. However, the laser on-state voltage is around 2 V and so there is a need for a higher supply voltage for the driver stage. It is possible to define two voltage domains: 0.9 V ($VDD_1$) and 2.5 V to 3 V ($VDD_2$). The total targeted power dissipation for the transmitter is around 1 mW/(Gb/s). This power should decrease once the link speed decreased and vice versa. In the design phase the optimum power for each targeted bit rate would be approximated and all the driver circuitry bias points would be programmed for different speeds.

One note is that the link speed actually changes during operation and the power of the driver should also change accordingly. At the moment the plan is to stop the data to the driver, update the bias currents of the circuitry to accommodate the new link speed, and then start the data stream again. Due to this process, the turn-on time is of very high importance and cannot be neglected. One scenario is that the driver circuitry goes to low power mode instead of being turned completely off.

A summary of the targeted parameters and specifications for the LDD is listed in Table 6.

**Table 6: Summary of targeted VCSEL driver specifications.**

| Parameter | Min | Max | Unit | Remarks |
|---|---|---|---|---|
| **Bias current** | 0.3 | 8 | mA | |
| **Modulation current** | 4 | 8 | mA | |
| **Supply voltage (driver)** | 2.5 | 3 | V | |
| **Supply voltage (digital)** | 0.8 | 1.2 | V | |
| **Power** | tbd | 60 | mW | Adaptive |
| **Bit rate** | 7 | 56 | Gb/s | Adaptive |
| **Turn-on time** | tbd | 10 | ns | |

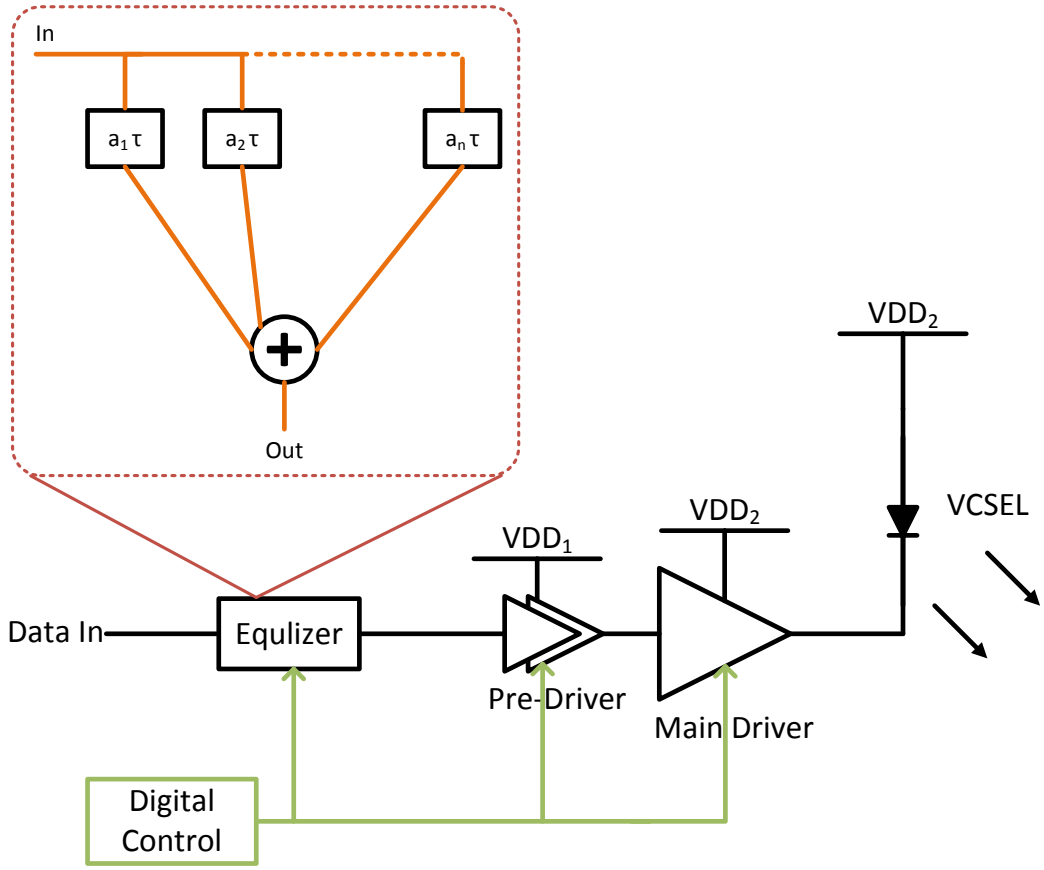



**Figure 8: An overview of the transmitter chip.**

### 4.2.2 Additional circuitry

In the prototype circuit including one link path, TX data will be generated by an internal sequence generator clocked at 1/16 rate, corresponding to 3.5 GHz.

A power up/down sequence is controlled by a digital engine which receives the power up/down signal from an external pin. At power up, the sequence generator outputs a preamble sequence for CDR locking followed by a programmable PRBS sequence. The 16 bit words are then serialized to full rate before being sent to the laser-diode driver (LDD).

## 4.3 *Receiver ICs*

### 4.3.1 Transimpedance/limiting amplifier

The purpose of the analog front-end of the receiver chip is to capture the photocurrent from the photodiode and amplify it into a voltage signal required for the CDR. Because of this conversion, the key circuit of the analog receiver front-end is called transimpedance amplifier (TIA). Due to the low amplitude of the photocurrent, it is generally not possible to reach sufficient signal level with only one stage TIA. Therefore, the analog front-end is complemented by a chain of voltage amplifiers.

Additionally, it is a good practice to stabilize the output amplitude over a larger span of input photocurrent values. This reduces the effect of the photodiode on the output signal value. The variation of the photocurrent amplitude can be caused by a variety of influences such as photodiode aging, production tolerances, different length of the optical link, misalignment of the optical fiber and detector during assembly. The limiting amplifier (LA) stage is responsible for the stabilization of the output signal.

A mismatch caused by production tolerances can result in a shift of operating points. To prevent this, a low-frequency feedback loop may be included into the optical front-end as well. As the basis of the feedback loop, there is a low pass filter (LPF), so that only the DC component is subtracted at the input and AC components remain unaffected.

The final optical front-end subsystem therefore consists of a TIA, multiple amplifier stages, a LA and feedback loops as shown in Figure 9. Besides the components, also the major parasitic effects are included into the schematic. These are the pad capacitance $C_{pad}$, and the bondwire inductance $L_{bond}$. $C_{pad}$ is caused by the bonding pad on the chip and the wiring between the pad and the TIA. Its value is estimated to 40 fF. The $L_{bond}$ is created by a bondwire connecting the photodiode to the receiver chip with estimated value of 300-500 pH.

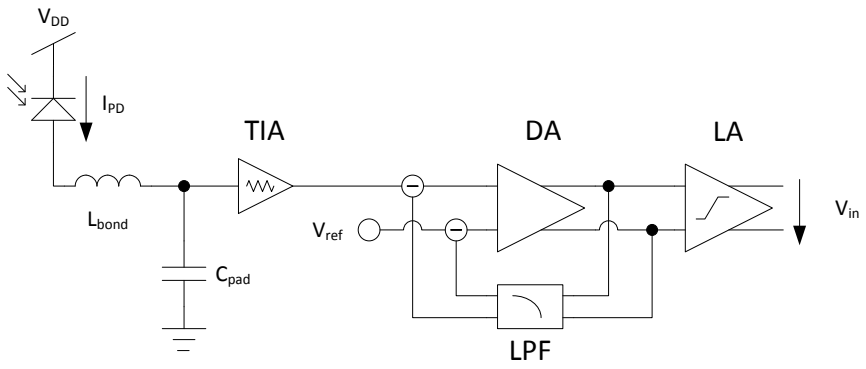



**Figure 9: Optical front-end subsystem.**

The analog front-end has to fulfil several requirements. First of all, the amplification of the signal has to be sufficient for the subsequent CDR, to recognize the transmitted information. For this, differential voltage swings of 100-150 mV, corresponding to the amplitude of 50-75 mV, are required. The estimation of the photocurrent is based on the optical budget. With common values of coupling efficiency and VCSEL power limited to 1 dBm due to eye safety regulations, the optical budget results in values of -12 to -9 dBm of optical modulation amplitude (OMA) at the receiver. This corresponds to photocurrent amplitudes of 16 µA and 32 µA, respectively. Therefore, a minimum transimpedance gain of 5 kΩ is required. This value is further increased by the requirement of limiting behavior, resulting in practical design target in the order of 10 kΩ. The gain of a single stage TIA usually reaches 200-250 Ω and a wideband differential amplifier stage a factor of 2. Therefore, it can be assumed, that the front-end will have to contain approximately 6 differential amplifier stages in addition to the TIA.

Second, the analog front-end has to possess sufficient bandwidth to process the input signal. The bandwidth of the optical front-end is predominantly defined by the input pole of the TIA. The input resistance of the TIA in combination with the capacitance of the photodiode defines a first order low-pass element. The capacitance of the photodiode with both bond pads larger that the transistor capacitance on the chip. Therefore, this pole occurs at lower frequency than the other poles and defines the system bandwidth.

The bandwidth required for a certain data rate is not defined precisely. Instead, the bandwidth to data rate ratio defines a trade-off between two major noise contributors. Low bandwidth reduces also the width of the noise spectrum by filtering out high frequency noise components. Therefore, low bandwidth of the front-end reduces random noise power. On the other hand, low bandwidth increases the response time of the circuit. The transient of a symbol does not settle before the arrival of a next symbol. The transients of multiple signals are partially superimposed at the output resulting in an inter-signal interference (ISI). Opposite to the white noise, this effect is deterministic. In general, 0.7 times the data rate is considered as a good trade-off between the noise power and inter-symbol interference (ISI). However, this value does not consider measures mitigating the ISI. Because the ISI is a deterministic effect, the signal can be reconstructed using the knowledge of previous symbols and subtracting their influence. This operation is called decision-feedback equalization (DFE).

The noise power accumulated over a bandwidth of 40 GHz might be too high in comparison to low amplitude of the received signal. Assuming the average spectral current noise of $20\ pA/\sqrt{Hz}$, as common in literature [22], the integrated noise results in an input referred noise of 4 µA. This noise value would not allow optical input signals below -9 dBm. Besides, the bandwidth of 40 GHz may be hard to achieve even with the newest CMOS technologies. Therefore, a more feasible approach is to deliberately reduce the bandwidth below the bandwidth-to-data rate ratio of 0.7. This leads to a reduction of the white noise at the cost of increased ISI. DFE is used to reconstruct the signal by subtracting the influence of previous symbol. Thus, it is possible to reduce the noise power considerably as well as relax the bandwidth requirements. A system level simulation of analog front-end and CDR is required to verify the impact of the DFE on the ISI. These simulations require accurate assumptions about the behavior of the analog components and therefore, have to be postponed until a coarse design of the analog front-end has been finished.

The power consumption of the analog front-end has to be kept at minimum with regards to the energy efficiency. While measures can be taken not to waste power, a certain minimum power has to be invested to meet the requirements on gain, bandwidth and noise with available technology.

The consortium has agreed to place the priorities as following. First of all, the aim is to reach the data rate of 56 Gb/s. After that, the low power measures, including the adaptivity will be addressed. This determines in particularly the bandwidth of the receiver front-end. If the simulations confirm the function of a DFE as expected, the front-end can be designed with a bandwidth of approximately 20 GHz. Else, the bandwidth will have to be increased above 28 GHz, where the ISI is still acceptable. The gain of the front-end is given by the threshold requirements of the CDR. As amplitude of 50-75 mV is required, the transimpedance gain of the complete front-end should be 8-10 kΩ or 78-80 dBΩ. Because it has been decided to prioritize the performance, the power

requirement will result from the design. As a reference, the energy efficiency of 0.5 pJ/bit has been decided, which corresponds to a power consumption of 28 mW. The target parameters are summarized in the Table 7.

**Table 7: Target parameters of the analog receiver front-end.**

| Parameter | Target value | Unit | Comment |
|---|---|---|---|
| Bandwidth | 20 (with DFE)<br>28 (without DFE) | GHz | To be determined by system simulations of the DFE |
| Transimpedance gain | 8-10 (78-80) | kΩ (dBΩ) | |
| Power consumption | 28 | mW | Soft target |

For the TIA design, a resistive feedback inverter has been chosen. This topology possesses an excellent compatibility with the technology. It is based on a standard digital inverter, with feedback resistor $R_F$ between the input and the output node, as shown in Figure 10. Therefore, it can be easily connected to a power grid. It also benefits from processing optimizations aimed at digital circuits, which are the main target of the technology and therefore more likely to occur. Besides, already present parameterized inverter cells can be reused with minor adjustments, reducing layout effort. This is a major advantage in sub 20-nm-technologies, where the layout complexity is much higher compared to older technology nodes. This topology has also been proven very effective by previous designs both in IBM and other groups [23], [24].

One of the advantages of the inverter based TIA is the well-defined operating point. Because of the feedback, the inverter is biased at equal input and output voltage. This is the metastable state of an inverter, where input voltage is equal to the output voltage and both transistors are in the pinch-off region. Due to the feedback resistor, this metastable state becomes stable. For symmetrical n- and p-MOS, this occurs at half supply voltage. In reality, the operating point is shifted slightly due by different current factors $\beta_{n/p}$ and W/L ratios of the n-MOS and p-MOS.

The input resistance of the TIA is minimized in order to compensate for the input load presented by the capacitance. In a feedback inverter topology, the feedback resistance is transformed to the input by the amplification of the inverter. Therefore, the input impedance $Z_{in}$ can be calculated as [25]:

$$Z_i = \frac{\frac{1}{r_{DS}} + \frac{1}{R_F}}{\frac{1}{R_F}\left(g_m + \frac{1}{r_{DS}}\right)} = R_F \frac{1 + \frac{r_{DS}}{R_F}}{1 + g_m r_{DS}}$$

and the amplification of the TIA is [25]:

$$Z_{tia} = \frac{g_m - \frac{1}{R_F}}{\frac{1}{R_F}\left(g_m + \frac{1}{r_{DS}}\right)} = R_F \frac{g_m r_{DS} - \frac{r_{DS}}{R_F}}{1 + g_m r_{DS}} \approx R_F \,.$$

These equations show that while it is necessary to increase the resistance $R_F$ in order to achieve higher gain, the value cannot be chosen too high as it would limit the bandwidth of the TIA. The simulations have indicated suitable values of $R_F$ to be in the order of 250 Ω.

Differential pair voltage amplifiers exhibit excellent behavior in terms of supply noise rejection. Therefore, a differential pair structure shown in Figure 10 has been chosen for the voltage amplification chain. A major challenge of the voltage amplifier is maintaining the bandwidth. Each additional stage causes further bandwidth reduction. Therefore, inductive peaking has been used to boost the bandwidth of the amplifier. In the final design, the inductance will be realized using active inductors instead of peaking coils in order to conserve chip area. For inductive peaking, for instance p-MOS common source circuit load can be used.

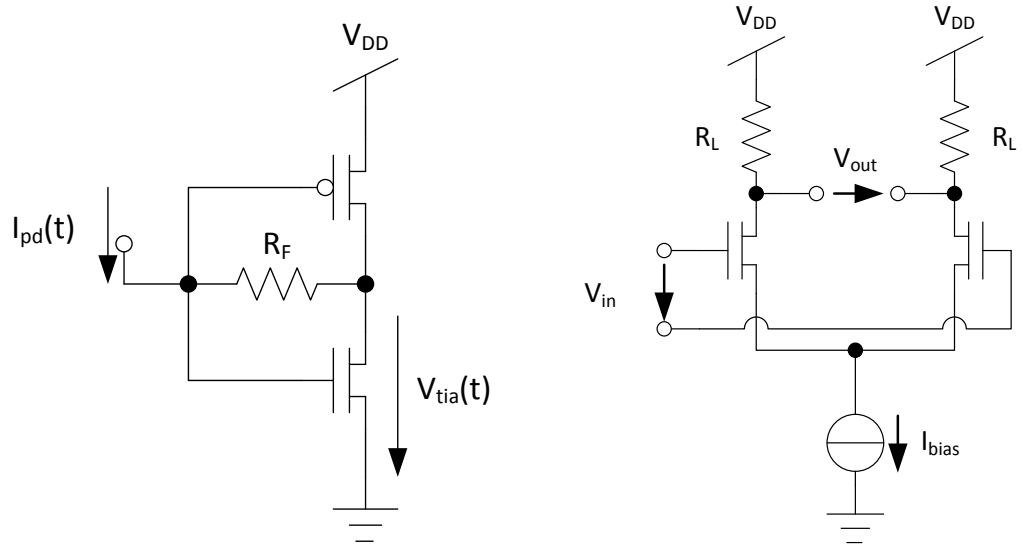



**Figure 10: Schematics of an inverter-based TIA with resistive feedback and differential amplifier.**

The differential structure of the voltage amplifier requires two voltage inputs. On the other hand, the photodiode and the TIA are single ended. Therefore, it is necessary to provide conversion from single-ended to differential signal. The simplest way is to provide a reference voltage for the first differential stage. There are multiple ways to generate the reference. It can be generated from the TIA output using a low pass filter (LPF). Two major issues of the LPF approach are long settling time and issues with long sequences. Therefore, this approach is not suitable for adaptive circuits. Another option is to generate reference voltage using a DAC. While this approach is power efficient and simple, it tuning and adjustments may be needed to eliminate production tolerances. The most power hungry approach is using a dummy TIA. This approach is well suited for the inverter based TIA, as the operating point is well defined. As a result, this topology is effective in suppressing process tolerances. If the connection between TIA and dummy is low-ohmic, it is also possible to eliminate supply noise with this structure.

The amplifier chain is terminated by a voltage limiting stage. This stage is also based on the differential amplifier topology. The bias current is however strongly reduced, in order to reach saturation for input peak values.

For the final design, additional feedback loop will be required in order to eliminate the mismatch between both signal paths. A well designed feedback loop can also eliminate the need for a dummy TIA, contributing to power reduction. On the other hand, the feedback loop does not suppress supply noise at the TIA, unlike a dummy stage.

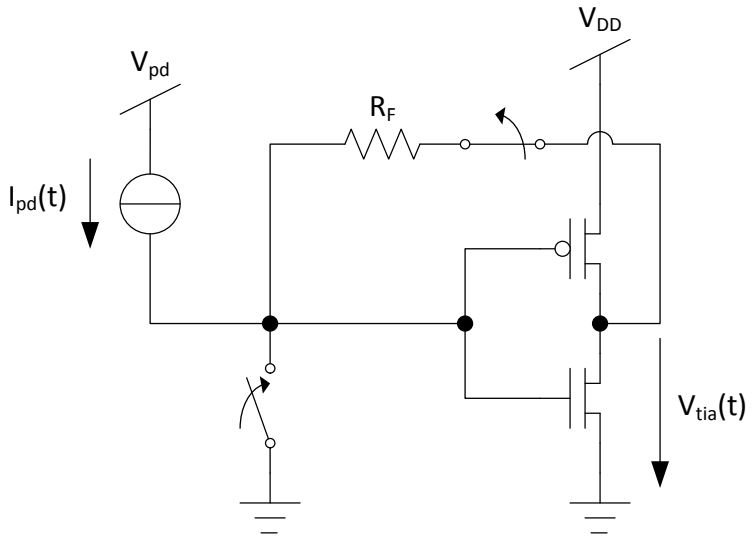



**Figure 11: Inverter Based TIA with on-/off adaptivity.**

Two types of adaptivity are required for the circuit. First, the design should be capable of fast on-/off-switching. The individual links will be activated and deactivated within nanosecond timescale to save power according to link utilization. This can be achieved by simply pushing the photodiode output below inverter threshold. The current source sinking the quiescent current from the photodiode can be reused for this. Below the decision threshold, the n-MOS of the inverter is switched-off resulting in negligible power dissipation. The current flowing through the feedback resistor has to be prevented. Therefore, a switch will be added into the feedback branch in order to break the feedback. The corresponding schematic is shown in Figure 11. The differential amplifiers can be switched off by controlling their biasing current source. The second adaptivity mechanism is bandwidth adjustment. This means that bandwidth and power can be traded off during operation. Because the circuits, and most importantly the CDR, will have to settle during the adjustments, this adaptivity mechanism will require longer settling time. Therefore, this mechanism is suitable to adapt the link to slower utilization fluctuations, such as periodic data transfer variations during the day. This adaptivity mechanism will be slightly more challenging to introduce. In the differential and LAs, the current sources can be modified into simple DAC structures. This can then be partially or completely switched off and comply with both adaptivity concepts. On the other hand, this adaptivity mechanism is rather challenging for the inverter-based TIA. One of the possible solutions is to extend the inverter into a cascode inverter and use the bias voltage for the adaptivity. Another option is to use an external voltage regulator to adjust the supply voltage. While an external voltage regulator requires rather long settling time, the power efficiency is much higher than with on chip regulators. Besides, the time delay of the regulation is not critical for the intended adaptivity.

So far, a TIA, differential amplifier and limiting stage have been designed for operation at 25 GHz. Lumped component models of these blocks will be prepared for a system level verification of the DFE mechanism. Depending on the results of the simulations, the bandwidth will be adjusted to maximize the benefit of the DFE. Besides, additional enhancement techniques will be tested, such as using cascode differential amplifiers to reduce Miller capacitance and improve differential amplifier bandwidth. Next, a feedback loop will be designed to control the operating point of the amplifier chain and eliminate possible mismatch. Finally, switches will be added into the design to enable adaptivity.

### 4.3.2 Clock- and data-recovery

The 56 Gb/s serial data stream fed by the analog front-end (AFE) gets sliced and converted to binary levels. The CDR aligns the RX clock to the middle of the data eye and tracks any frequency offset between the TX and RX macro within a specified rage. In the frame of the ADDAPT project, fast CDR locking is a key requirement to wake up the link within the 20 ns allocated budget.

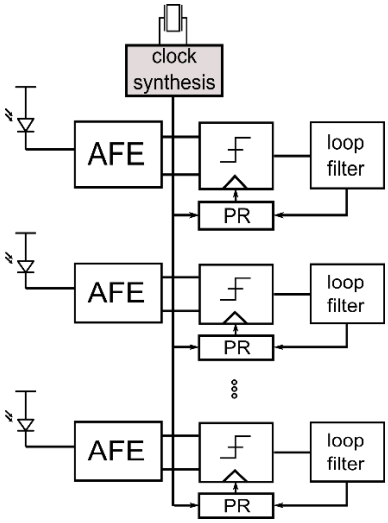



**Figure 12: Embedded clock optical link with reference clock.**

Figure 12 depicts the embedded clock (EC) link architecture with reference clock envisaged for the adaptive optical link. The RX CDR macro is a dual loop architecture consisting of three functional sections: a frequency synthesizer, a phase rotator (PR) and CDR loop filter. The frequency synthesizer generates the target clock frequency with a LC-VCO PLL from a low frequency reference clock, (around 100 MHz), typically implemented with a crystal oscillator. This scheme is advantageous since the frequency synthesis can be shared among many links, reducing power and improving area efficiency of the overall transceiver. A digitally programmed PR then finds the optimal sampling position interpolating among a set of discrete phases. The PR block is driven by a digital CDR loop filter. A digital CDR loop results in a compact and power efficient design. A digital implementation of the CDR offers many advantages. Namely, 1) substantial PSRR noise sources in the analog control loop are absent in the digital implementation; the PR is the only mixed component, which is locked to a quit reference clock, allowing the choice of higher loop bandwidth,

2) the performance of the loop is derived through its digital functionality rather than by sensitive analog components and 3) ease of allowing flexible control of design parameters.
The architecture of Figure 12 uses two different reference clocks on TX and RX side that may not have exactly the same frequency output. Hence, the PR needs to align both the phase and frequency of the incoming data. The frequency misalignment can be corrected constantly rotating the PI phase output to emulate a frequency shift.

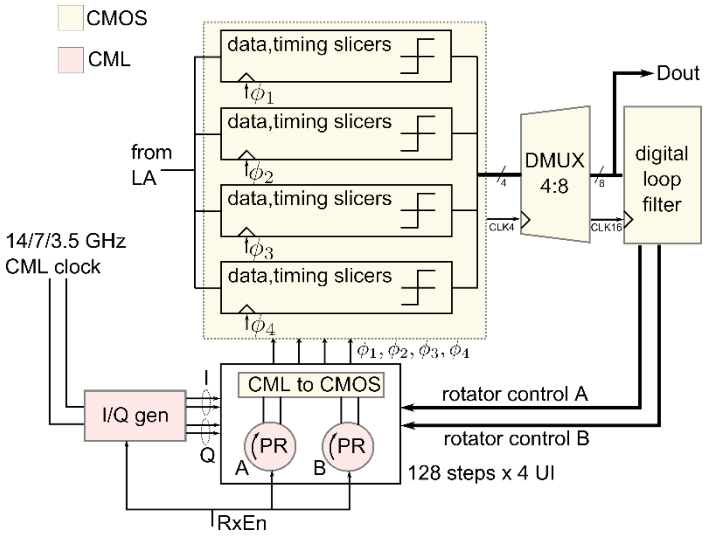



**Figure 13: CDR Block diagram. The bias current of PRs and I/Q generation can be turned off to save power while the link is idle.**

Figure 13 shows a detailed view of one link path CDR which will be submitted for fabrication in the 4th quarter of 2014. The circuit uses a four-phase design where each slice operates at quarter rate. This allows clocking the RX with four quadrature phases at ¼ of the data rate (14 GHz for 65 Gb/s data rate), thereby relaxing the requirements of the sampling latches and the clock distribution circuits. Moreover, spreading the current among four slices makes it easier to fulfil electromigration requirements.
Quarter rate binary data are demultiplexed to octal rate (8 GHz) and fed to the digital 2nd order loop filter which drives the digitally programmed PR.
Phase rotation is implemented with a four quadrant CML mixer which provides 32 steps per UI interpolating I and Q differential phases. I/Q generation consists of a CML divider. Since each rotator generates a differential output signal, two PRs in parallel are required to generate the 4 single ended clock phases feeding the clocked comparators.
Unlike previous CDR architectures, that use 2X oversampling, a baud-rate rate sampling scheme is used to capture the data as well as generate an error signal from the center of the data eye for driving the timing. Hence, the extraction of timing information requires an additional sampler in each RX slice. This technique is the most effective approach in terms of power and area since does not require an extra PR to generate edge samples.
The CDR macro can be powered on/off by means of an external trigger signal (RxEn). The primary adaption mechanism in ADDAPT project consists of rapidly switching on/off link paths as a

function of network traffic. In the proposed CDR implementation, the CML circuits, namely the PR and frequency divider can be switched by shutting down the bias current. As a consequence, the CMOS section no longer receives the clock signal and therefore does not consume any dynamic power. A complete switch on/off characterization will be provided by measuring the RX prototype implementing one link path.
Interestingly, the CDR energy efficiency improves at lower data rate by reducing the supply voltage of CMOS circuits. Hence, speed throttling is considered as a secondary power saving approach. Therefore, one link path will be characterized at different data rates (56, 28, 14, 7 Gb/s) to assess the power saving opportunity with per link speed adjustment. It should be noted that supply voltage scaling is a slower process with a time constant in the µs or even ms range.
Table 8 reports the specification of the CDR circuit for the upcoming chip submission.

**Table 8: CDR Specification for one link path.**

| Parameter | Value | Unit |
|---|---|---|
| Data rate | 56 – 28 – 14 - 7 | Gb/s |
| Energy efficiency @ 56 Gb/s | 2.5 | mW/(Gb/s) |
| Lock time | 10 | ns |
| Input signal level | 100-150 | mV |
| Common mode range | 650-750 | mV |
| Frequency offset | ±100 | ppm |

### 4.3.3 Additional circuitry

To simplify measurements and enable a complete characterization of the RX macro additional circuit blocks will be added to the basic RX functionality. Namely, a PRBS checker running at octal rate will lock to a PRBS sequence and count the received error. BER measurements as a function of a given CDR lock time provides a direct measurement of minimum time required to power up the link and achieve error free operation. Moreover, on die scope capability will be also provided. Hence, the RX eye diagram can be synthesized sweeping the PR setting and scanning the eye vertically at each PR step. Finally, a digital block responsible of turning on the link path as a function of an external trigger signal will be also implemented. All of those circuits and all CDR parameters will be controlled by an IBM proprietary serial interface which can be interfaced with an FPGA or a microcontroller unit.

# 5 Conclusion

In this report the initial concepts and the specifications of the ICs for the ADDAPT electro-optical transceiver are described. The main circuits involve LDD, TIA/LA and CDR. The initial concepts and specifications are derived by considering the potential adjacent aspects such as potential applications, the system concept, the optical components and the assembling/packaging approaches. Goals for the circuit design are high speed with data rates up to 56 Gb/s, high energy efficiency and low power consumption in the order of a few pJ/bit as well as performance and power adaptivity. Adaptivity will be enabled by rapid switch on/off with switching times <20 ns and bandwidth tuning to enable scaled data rates of 56, 28, 14 and 7 Gb/s. An initial simulation has shown that by reducing the bandwidth to 30-50 % of the peak bandwidth, the power consumption can be reduced by 50 %.

The circuits are designed in a 14 nm CMOS technology. In addition, optional 28 nm runs will be used to investigate and evaluate for example basic adaptivity approaches. For the LDD a pre-emphasis or equalization has to be implemented in order to overcome the bandwidth limitation of the VCSELs. Therefore, a VCSEL model development is already in progress. The TIA has to have a high sensitivity, high gain and low noise. The high-speed CDR has to enable a fast locking to guarantee the wake up of the link within the 20 ns.

A first 14 nm tape-out and fabrication is planed at the end of 2014. The next deliverable report D5.2 of WP5 will contain more detailed information about the design of the transceiver ICs. D5.2 will be available by project month M21 which is in July 2015.

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## Acronyms

| Acronym | Definition |
|---|---|
| AFE | Analog front end |
| BER | Bit error rate |
| CDR | Clock- and data recovery |
| CML | Current mode logic |
| DAC | Digital-to-analog converter |
| DFE | Decision-feedback equalization |
| EC | Embedded clock |
| IC | Integrated circuit |
| ISI | Intersymbol interferences |
| LA | Limiting amplifier |
| LC-VCO | LC-voltage controlled oscillator |
| LDD | Laserdiode driver |
| LPF | Low pass filter |
| OMA | Optical modulation amplitude |
| PR | Phase rotator |
| PRBS | Pseudo-random bit sequence |
| PSSR | Power supply rejection ratio |
| RX | Receiver |
| TIA | Transimpedance amplifier |
| TX | Transmitter |
| VCSEL | Vertical-cavity surface-emitting laser |
| WP | Workpackage |