ADDAPT

Adaptive Data and Power Aware Transceivers for Optical Communications

Deliverable D 1.1

PROJECT INTERIM STATUS REPORT

Grant Agreement number: 619197

Project acronym: ADDAPT

Project title: Adaptive Data and Power Aware Transceivers for Optical Communications

Funding Scheme: Small or medium scale focused research project (STREP),
FP7- ICT-2013.3.2

Date of latest version of Annex I against which the assessment will be made: 2013-09-03

Period covered: from 01.11.2013 to 31.07.2014

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Document information

Title	D1.1 - Interim status report
Work package	W1 – Management
Responsible	Technsiche Universität Dresden (TUD)
Due date	Project M09 (July 2014)
Type	Report
Status	Version 1.0
Security	Public
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Project URL	www.addapt-fp7.eu

Confirmation

Any work or result described in this report is either genuinely a result of this project or properly referenced.

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Version Management

Table 1: List of Revisions

Version	Description	Author	Released
V0	First setup; template	R. Henker (TUD)	July 23, 2014
V01	Input Section 2.2.2	M. Georgiades (PTL)	July 30, 2014
V02	Input Section 2.2.5	M. Zoldak (AT)	August 5, 2015
V03	Input Sections 2.2.3	J. Kropp (VIS)	August 14, 2014
V04	Input Sections 2.2.1	P. v. Leeuwen (TE)	August 14, 2014
V05	Input Sections 2.2.2	T. Toifl (IBM)	August 18, 2014
V06	Input Sections 1, 2, 2.2.4, 2.3, 3	R. Henker (TUD)	August 29, 2014
V1	Final revisions	R. Henker (TUD)	September 03, 2014

1 Publishable summary

The performance requirements of existing and future optical networks, especially of the optical links and interconnects, are not static and change over time. The individual needs of the users, applications and boundary conditions lead to a strong dynamic behaviour of data rate in today's data networks for instance. However, existing optical networks operate statically at their maximum performance to accommodate the peak traffic requirements and therefore, do not offer much adaptability. Thus, the links are not energy-efficient. The networks and their system components have to be able to flexibly reset to those changes. Therefore, one of the main innovations treated by ADDAPT is to adjust the performance and in turn the power consumption of the multiple optical links from system down to optical device, electrical circuit and transistor level to the actual required data load and link conditions. To achieve this, a high-speed optical transceiver module will be developed whose parameters like bandwidth, modulation format, clock rate, amplitudes can be adapted. This leads to a flexible reconfiguration of the system according to the actual transmission requirement which in turn reduces the system power consumption at the same time. To realize this, a smart adaptivity control is implemented that decides how and when the system parameters need to or may change. The development of such an optical interconnect paves the way to build flexible energy-efficient optical transmission links and networks coping with varying bitrate demands and pave the way for massive reductions of CO_2 emission and costs.

The ADDAPT concept and project structure are shown in Figure 12 and Figure 13 of the Appendix. The focus is the development of a transceiver module and its components. This includes novel adaptive directly modulated lasers and photodetectors designed by VI Systems (VIS) and fabricated by Compound Semiconductor Technologies (CSTG) in III-V technologies for near-field light coupling to allow self-aligned low-cost waveguide assemblies with minimum optical power losses. Laser bandwidths beyond 30 GHz and power consumption can be traded off and controlled by driver circuits. Circuits such as amplifiers, drivers and clock-data-recoveries for high-speed data rates between 7 and up to 56 Gb/s and low power consumption, which can be adjusted via current sources, dc/dc converters, regulators and switches, are designed by IBM and TU Dresden (TUD) in energy-efficient 14 nm CMOS. High-speed, low-loss packaging solutions using glass or ceramics are developed by Argotech (AT) to build the transceiver demonstrator. An optical communication platform tailored for data centers is designed by IBM with 4 link paths and maximum 10 m link distance for verification of speed adaption from 0.224 Tb/s to 7 Gb/s with an overall power saving factors of up to 6 (if just one link is active and tuned to the lowest data rate). The measurements of the adaptive optical link based on the ADDAPT subsystems and transceiver module is performed at Warsaw University of Technology (WUT). The development of the transceiver is market, application and standard driven and accompanied with network analysis in a data center of PrimeTel (PTL) and market considerations by Tyco Electronics (TE). Therefore, ADDAPT combines the complementary competences of 3 large companies, 3 SMEs and 2 universities including device manufacturers, suppliers of communication equipment and network operators. Involved EU and associated countries are the Netherlands, Czech Republic, Poland, United Kingdom, Cyprus, Switzerland and Germany.

The primary goal of ADDAPT is to develop a high-speed electro-optical transceiver module with implemented performance and energy adaptivity on component level (optical devices, ICs) as well

as on system/module level. For this two basic methods are investigated: Depending on the actual data load, first, smart switching of the link paths and lanes (sub-paths of the link paths) allows step-wise (coarse) adaption by switching the complete link on/off or in a power down mode. Second, smart tuning allows continuous (fine) tuning of individual link paths and its components in their performance parameters such as bandwidth, clock frequencies, amplitude and gain by vary the supply currents and voltages of the devices. Several control types are investigated: cognitive adaption based on predetermined or time averaged loads and real-time adaption. Driven by control units including smart algorithms, the devices can be tuned from 7 up to 56 Gb/s while vary the power consumption. Although the decision and setting for the switching and tuning will be executed by a higher-level control system including software, the tuning of the performance and power consumption has to be realized inside the devices and components. Thus, the development of components with ability to adaption is necessary.

Scaling the power consumption of such transceiver subsystems, results in a significant reduction of the power consumption and operating costs of optical interconnects. To achieve this, the full supply chain from semiconductor technologies, component and system design over packaging, assembling and characterization to user requirements, interconnect applications and commercial markets is covered by the consortium. The project objectives can be summarized as follows:

- Low-cost power-efficient directly modulated surface emitting lasers (VCSELs, NFLs) and photodetectors (PDs) suitable for data transmission up to 56 Gb/s (up to 40 GHz bandwidth) with ability to reduce data rate while simultaneously reducing the power consumption
- Optional employment of pre-/deemphasize techniques for bandwidth enhancement
- Advanced techniques for light in- /out-coupling even at small apertures allowing smaller pitch size, costs and higher density of the interconnects
- Low power consuming transceiver ICs in 14 nm CMOS capable of tuning of possible data rates from 7 to 56 Gb/s to enable supply power reduction at lower data rates
- Several adaptivity control concepts based on cognitive, averaged and real-time workload information will be considered and benchmarked by intensive network load analysis
- Adaptive data rate and power scaling by smart switching of parallel link and lane paths
- Adjustment of performance, data rate and power trade-off by smart tuning of specific link paths
- Use of a control platform including algorithms and a data protocol to externally control the hardware components allowing adaptivity
- Enhanced packaging and assembling techniques (such as wire- and/or 3D flip-chip bonding) on glass or ceramics capable of HF electrical driving lines and data rates up to 56 Gb/s
- Verification platform with 4 link paths yielding up to 0.224 Tb/s at $\leq$ 10 m link distance
- Conceptual study for scalability and performance enhancement of the demonstrator up to aggregated data rates $\geq$ Tb/s e.g. by application of higher-order and multi-level modulation formats
- Assessment of the developed technologies (e.g. the adaptive ICs) for applications in other optical transmission areas such as long-haul transmission systems

The key application of the ADDAPT developments are seen in optical interconnects for short range data communication as used in data centers or high performance computing (HPC) for rack-to-rack,

server-to-server and board-to-board connections. One possible application would be to replace standard active optical cables (AOC) with fixed performance and power consumption by including the ADDAPTive transceiver. The impact of ADDAPT is the significant lowering of the power consumption of those optical interconnects and therefore, reducing significantly the operating costs and CO_2 emission of optical data communications systems and data centers.

In the reported project period, the following work has been performed and the following main results have been achieved:
In WP1 'Management' the project has successfully started and contractual issues regarding the Grant and Consortiums Agreements have been successfully finished. The pre-financing of the project has been distributed and transferred to the partners. The project is established and appropriate communication between the partners is arranged. The kick-off meeting and the second project meeting were organized. Furthermore, webconferences with all or just few project partners on a regular basis are scheduled and performed. A webpage is created and updated periodically to inform and promote the public about the project. A secured data sharing system is created which can be used to exchange information and documents among the ADDAPT partners. During the reported project period, 7 project deliverables with reports have been prepared and submitted.
In WP2 'Market studies, exploitation and dissemination, standardization' the performed work consists of: a) understanding the market and specification of ADDAPTive cables, b) how to exploit the results of the work done for ADDAPT, c) what standards are to be influenced as a result of insights learned developing the ADDAPT technology, and d) how to disseminate those results. It has been determined that the market for this technology is existing, the potential is huge (hundreds of thousands of cables), and is predominantly to be found in the high performance computing and datacenter environments. To implement the ADDAPTive approaches can only be achieved if the relevant standardization bodies adapt this technology in the various standards. All partners have clear ideas how to exploit and disseminate the insights, know-how, capabilities and products can contribute to the objectives of the various organizations. The results are summarized in the deliverable reports D2.2 and D2.3.
In WP3 'Network analysis, system design and verification platform' an intensive study on the system concept has been proceeded on the basis of the market and application review. Most suitable standards for the ADDAPT transceiver module seem to be Infiniband and Ethernet. The system concept consists of a 4 channel transceiver (one master and three slaves), each channel for data rates of up to 56 Gb/s, with high energy efficiency and equipped with adaptive rapid on/off switching and speed tuning functionality for additional power savings. For the bandwidth and power adaptivity of the transceiver a rapid switch on/off approach by detecting IDLE packets of the protocol (e.g. Infiniband) has been developed. For the smart adaptive tuning a change between different data rates (56-28-14-7 Gb/s) is considered. Furthermore, an intensive, long-term network analysis has been started which determines different network parameters and gives insights on the dynamic network behavior in micro- and macro-time scale.
In WP4 'Adaptive optical components' first concepts and specifications for optical components were stated and discussed which are summarized in the deliverable report D4.1. It is necessary to establish a close collaboration in the development of optical components and analog electronics which include equalizing functions to reach the goal of an adaptive optical connection with speed of

up to 56 Gb/s. Current optical chips are provided to the partners to derive new circuit models for the design of the analog electronics. Discussions about near field coupling (NFC) of the optical components were started but no verified concept exists today. Close collaboration of VIS and IBM will be started in the second half of 2014 about that subject.
In WP5 ‘Adaptive integrated circuits’ initial concepts and specifications for the adaptive transceiver ICs have been derived from different requirements (e.g. markets, applications, system concept, optical components, the assembling/packaging techniques) and summarized in the deliverable report D5.1. A high data rate of up to 56 Gb/s and a high overall energy efficiency of around 4 pJ/bit is targeted for the LDD, TIA/LA and CDR. Adaptivity in terms of on/off switching and bandwidth/power scaling is implemented into the circuits. The LDD involves equalization to enable high data rates in combination with a lower bandwidth VCSEL. Therefore, a VCSEL model development is in progress. The TIA should have a high sensitivity and low noise. The key functionality of the CDR is the rapid on/off switching below 20 ns. The IC design has been already started and is in an early state. A first tape-out and fabrication of the chips is planned at the end of 2014 containing a one lane transceiver sub-system for the verification of the high speed, low power consumption and rapid on/off switching functionality.
In WP6 ‘PCB and packaging’ the electrical interface has been concluded to be based on coaxial connectors in early stage of the project. Other options to utilize any pluggable interfaces for data transfer at 56 Gb/s at least for 4 lanes in parallel are under investigation. The HF design of demonstrator board/package has been heading to the end of its first iteration. The preliminary 3D FEM simulation results show the complete line insertion loss below 3dB (IC pad interface to coaxial connector interface). Furthermore, several packaging approaches and its dependences to HF signal transfer are investigated for demonstrator board/package. The optical link specification is under definition in terms of optical budget and all related parameters. It shows a low power margin and thus, several actions are planned to increase it.

A project website has been prepared which contains all relevant information and news about the project. It is updated periodically and can be accessed under http://www.addapt-fp7.eu/.

2 Core of the report for the period

2.1 *Project objectives for the period*

The objectives of the reported project period (November 2013 to July 2014) mainly involves the project launch and the initiation of the management structure and tools in the administrative part as well as the development of first concepts and specifications in the technical part of the project. The particular objectives of the several WPs can be summarized as follows:

- WP1 'Management'
  - organizing project launch
  - contractual management of Grant Agreement (GA) and Consortium Agreement (CA)
  - organizing financial issues, e.g. transfer of pre-financing
  - organization of project meetings (e.g. kick-off meeting)
  - organization and planning of communication among the partners, e.g. via webconferences, data sharing system, phone calls and emails
  - coordination of writing and submission of deliverables and reports (D1.1, D2.1, D2.2, D2.3, D4.1, D5.1, D6.1) including preparation of public project presentation and fact sheet
  - overall administration and risk management

- WP2 'Market studies, exploitation and dissemination, standardization'
  - Market study including review of potential existing and future applications and standards
  - determination and definition of requirements for the ADDAPT transceiver
  - organizing the plans for dissemination and exploitation of the project results among the entire consortium
  - evaluating ongoing standardization processes and figure out the possible actions out of ADDAPT
  - implementation and update of project website on a '.eu' domain
  - active dissemination via press releases and other public material
  - issue of deliverables and reports, e.g. D2.1, D2.2 and D2.3

- WP3 'Network analysis, system design and verification platform'
  - development of a system concept and architecture
  - determination and definition of system specifications including key components and interfaces
  - conceptional study of different adaptivity approaches and adaptivity control
  - consideration and study of data protocol
  - electrical and optical link budget
  - links simulations
  - performance of network analysis regarding different parameters on sort and long time scale

- WP4 ‘Adaptive optical components’
  - concepts and specifications for the design of the optical components
  - evaluation of fabrication processes for the high-speed optics
  - modelling of the optical components as basis for IC design
  - start of the optical component design
  - start of optical component fabrication
  - conceptual study of the NFC approach
  - issue of deliverables and reports, e.g. D4.1

- WP5 ‘Adaptive integrated circuits’
  - concepts and specifications for integrated circuits including consideration of optical devices, interfaces etc.
  - enable technology access and arrange IC design platform
  - evaluation of technology performance
  - study and development of different adaptivity approaches
  - evaluation and development of different circuit topologies for the key transceiver ICs
  - start of receiver and transmitter IC design
  - issue of deliverables and reports, e.g. D5.1

- WP6 ‘PCB and packaging’
  - packaging concept and interface definition for sub-systems and verification platform
  - evaluation of different substrate materials, of electrical and optical connections
  - evaluation of different bonding types for chip-to-chip and chip-to-board concretions
  - HF simulations on board and interface level to determine signal losses and cross talk
  - start of the packaging technique development
  - issue of deliverables and reports, e.g. D6.1

At the moment there is no summary of recommendations from previous reviews available. A first project review of the first project period will take place in the first quarter of 2015.

2.2 *Work progress and achievements during the period*

2.2.1 WP2 Market studies, exploitation and dissemination, standardization

Introduction and objectives of WP2

WP2 is focused on generating insights for the market-oriented system and component based on market research. The focus was on understanding the area of transceivers for optical interconnects that benefit from the ADDAPT transceivers. This task has been driven by the industry partners who are specialists in the areas of device design and manufacturing, network and communication equipment supply, and network operation. The result of this is published in report D2.2.

Furthermore, based on those insights, this WP2 addresses how the ideas, products and components, know-how and capabilities are to be made available to the world at large, and how the European

community benefits from this. A first inventory of ideas for the exploitation and dissemination activities of the project has been made. The result of this is published in report D2.3
At the end of the project, a "dissemination kit" will be produced which contains suitable material (e.g. texts and pictures including copyright clearance). Given the phase of the project, this activity is not yet considered relevant.
Based on gained technical insights, this WP2 is also addressing standardisation. It has already been concluded that some particular networking standards have to be influenced to fully benefit the energy savings potentials of ADDAPT technology.
A web site is to be created on a ".EU" domain.
Leader of WP2 is TE.

List of involved partners and assigned tasks inWP2

In WP2 4 different tasks are defined:
T2.1 Market Study: The market analysis should reveal market aspects, applications and use-cases in the area of transceivers for optical interconnects that benefit from the ADDAPT transceivers.
T2.2 Exploitation: This is about how to exploit the technical results, such as, discussions with potential customers, product launches after project finalization, intellectual properties and patents, and derivative start-up companies.
T2.3 Standardization: Standardization issues and technical guidelines, active standardization processes and evaluation ADDAPT transceiver suitability, active participation in standardization actions.
T2.4 Dissemination: Activities such as web page on a ".EU" domain, workshop(s) for efficient dissemination of results and knowledge, joint scientific publications, student colloquiums, educational perspective into practice, press releases, technical events/conferences/exhibitions etc.

Table 2: WP2 involved partners

Partner	Task
Argotech (AT)	T2.2/T2.4 Supply of input with respect to exploitation & dissemination of knowhow and capabilities related to near field coupling, packaging and assembly in the 56 Gb/s domain and higher
Compound Semiconductor Technologies (CSTG)	T2.2/T2.4 Supply of input with respect to exploitation & dissemination of products and capabilities to design and fabrication of high speed VCSELs and Photodiodes in collaboration with VIS
International Business Machines (IBM)	T2.1. Supply of input with respect to supercomputing and datacenters. T2.2/T2.4 Supply of input with respect to exploitation and dissemination of technology in the domain of high speed SERDESs, low cost/high speed optical connection between ICs, and low power optical cables
PrimeTel PLC (PTL)	T2.1 Supply of input with respect to network behavior and applications and trends. T2.2 / T2.4 Supply of input with respect to the exploitation and dissemination of knowhow and means gained during this project in reducing CAPEX and OPEX, and by improving and extending its

	services and service portfolio.
TE connectivity	T2.1 Coordination of work, generation of report, performing market research on possible application of the system, organization of review T2.2 / T2.4 Coordination of work, generation of report, collecting input from Partners, organization of review
Technische Universität Dresden (TUD)	T2.2 / T2.4 Input with respect to Dissemination and Exploitation of knowhow in the domain of high-speed/broadband integrated circuits, IC design techniques, adaptive IC design techniques, device modeling, design, simulations and measurements. Provision and Maintenance of the ADDAPT website.
VI Systems (VIS)	T2.2 / T2.4 Input with respect to dissemination and exploitation in the domain of design high speed VCSELs and photodiodes.
Warsaw University of Technology (WUT)	T2.2 / T2.4 Input with respect to dissemination and exploitation in the domain of design high speed testing and characterization of optical components and systems, up to speeds of 56 Gb/s.

Executive summary of WP2 work and results

WP2 can be summarized as work addressing:

1. understanding the market and specification of ADDAPTive cables,
2. how to exploit the results of the work done for ADDAPT,
3. what standards are to be influenced as a result of insights learned developing the ADDAPT technology, and
4. how to disseminate those results

We learned this period (November 2013 up to July 2014) that the market for this technology is existing, the potential is huge (hundreds of thousands of cables), and is predominantly to be found in the high performance computing and datacenter environments.

A new insight is that the implementation gets easier, and the efficiency higher, if part of the ADDAPT technology will be implemented in the NIC. This leads also to the insight, that this can only be achieved if the relevant standardization bodies adapt this technology in the various standards. IBM and TE will pursue this in the standardization body where they are a member of.

Also, from a dissemination and/or exploitation point of view, we feel the development of a 12 lane demonstrator does not contribute to the acceptance of this technology. A 4 lane demonstrator does the same, having a clear focus on the key aspects of ADDAPT that it should demonstrate.

All partners have clear ideas how to exploit and disseminate the insights, know-how, capabilities and products can contribute to the objectives of the various organizations.

Detailed work progress and achievements

- T2.1 Market study:

  Task description: At the project beginning the market analysis should reveal market aspects, applications and use-cases in the area of transceivers for optical interconnects that benefit from the ADDAPT transceivers. This task is driven by the industry partners who are specialists in the areas of device design and manufacturing, network and communication equipment supply, and

network operation. Especially, data centers, HPC and computing clusters and core networks are considered as potential application fields. As one unique property the performance/adaptivity concept is taken into account. This investigation includes the identification of application areas, business models and opportunities as well as potential customers. With the feedback from the technology development and the market aspects, requirements for the system front-end will be investigated and specifications for products will be identified. Moreover, existing applications and standards in the market are considered together with a competitive technology analysis. Regarding to up to date market potentials, global issues for products and associated international research, this analysis will also include marketing and exploitation strategies for the results of ADDAPT. Competitive transceiver technologies and architectures will be used as benchmark.

Progress and results: This chapter is an extract of the report D2.2, market study, evaluation of application and product specification. It touches briefly upon the application markets for ADDAPT technology, addresses briefly the issue of network protocols, and then focusses on volumes for the various markets.

Applications

The envisaged market being addressed by ADDAPT is two-fold:

- High-capacity inter-switching (as in data-centers)
  - intra-rack communication
  - rack-to-rack communication
  - co-location communication
  - communication to storage devices.
- Supercomputers (HPC)
  - inter-processor communication
  - communication to storage devices

Both markets (data-centers and supercomputers) are be elucidated in a separate chapter of report D2.2.

Requirements for ADDAPT technology in data-centers

The envisaged protocols where ADDAPT might be relevant are:

- Ethernet, including various flavors of Ethernet. All these versions are targeting the data-center space. On top of that, various interfaces are developed to enable Ethernet over SDH. Those are targeting the telecommunication between data-centers.
- Infiniband
- Proprietary protocols in the HPC space, such as SMP (IBM), IQP (Intel), Gemini and Aries (Cray) and Tofu (Sparc). Those protocols have in common that they particularly have high bandwidth, RDMA and low latency.
- PCIexpress

Market Volume ADDAPT cables for data-centers

Ethernet inside the data-center is believed to be the most important application for ADDAPT cables, because it as more uniform than HPC cables (see above).

Table 3: Potential market for Ethernet ADDAPT cables

Protocol	Market
10 GbE	It can also be noted that the market for 10 Gb/s Ethernet Server Ports is really huge until 2016 (like 15 mill ports/year for server only) afterwards fast declining. It shall be investigated if 10 Gb/s is still an option for ADDAPT technology. If we can make it cheap enough, due to the volume, the potential power savings are huge.
40 GbE	This diagram suggests a potential market of 5 mill ports in 2016. The market will start to pick up per 2015.
100 GbE	The market for 100 Gb/s will definitely exist. Volume is expected to pick up per 2018 with a volume of several 100ds of thousands.

In other words, there is a potential market of approximately 6 million ADDAPT cables in the Ethernet world.

Communication between data-centers (co-locations)

For reasons of Point-of-Presence, security and backup, data-centers may want to communicate their data to co-locations. There are two basic ways the market is implementing this:

- Using a dark fibre, with an ADDAPT implementation of one of the relevant protocols.
- Connecting to a telecom standard interface, provided by a telecom provider.

We expect there is a (small) niche market for ADDAPT technology in the cables interfacing between the Ethernet router, and the SDH public interface.

Market for supercomputing

This is modelled around the IBM Power7 architecture. By extrapolating this to the supercomputing community, we found a potential market of

# in Million cables	50 cm	100 cm	2 – 10 m	totals
PCIe / SAS		1.3		1.3
SMP (IBM proprietary)	0.8	2.7	1.8	5.3
Proprietary + Ethernet + infiniband	2.4	6.4	4.3	13.1

Deviations: There are no deviations from plan, however, we feel the market study and requirements might need some updates over time as insights in functionality and applicability

grows. Especially the assessment of the market for supercomputing needs to be improved, it is too much modelled to the Power7 architecture.

Corrective Actions: As reported in 'deviations' we feel the market study could be improved. Every 6 month we will reconsider this report D2.2, and update where progressive insights give reasons to do so. Particularly address the supercomputing market more precisely.

Outlook: Keep on monitoring market developments, and

1. Deepen the market insights
2. Improve specification points accordingly.
3. Update the D2.2 report accordingly

- T2.2 Exploitation:

Task description: In this task the exploitation activities are organized. These can involve:

- First discussion with potential customers
- Preparation for product launches after project finalization
- Consideration of intellectual properties and patents
- Considerations for the funding of start-up companies (e.g. initiated by TUD)

Progress and results: The Exploitation plan is reported in the "Deliverable Report D 2.3, Plans for dissemination and exploitation of results". All partners have clear ideas how the insights, know-how, capabilities and products can contribute to the objectives of the various organisations.

The result can be summarized as follows.

Table 4: Exploitation plans per partner

Company	Exploitation
AT	Argotech expects deploy its position as a European provider of Manufacturing Services and Design Services in the area of high speed packaging of microelectronics and optoelectronics components.
CSTG	In addition to a primary partnership with VIS, CST will also offer a generic chip manufacturing platform to third party OEM component vendors as an extension to existing foundry process for <10G VCSELs. This process will be tailored to individual device needs (e.g. specific epitaxial wafer structures, device geometries, custom optoelectronic specifications etc.) for a wide range of custom applications.
IBM	IBM expects to remain the leading supplier for cloud data centers and high-end computing, which will result in a large number of produced P- and Z- processors and associated systems using several tens of millions of optical connections. The SERDES IP blocks will enable ASIC customers to develop there chips with unprecedented bandwidth requirements with IBM.
PTL	ADDAPT's results will enable PrimeTel to upgrade its telecommunication and

	data services. This will allow PrimeTel to attain strategic as well as economic gains, meet increasing customer needs in terms of increased bandwidth at lower prices, remain competitive and ultimately promote novel business opportunities. Examples are an IPTV service (PrimeTV) and HD video streaming, and fast access to data and storage cloud facilities. Moreover, ADDAPT will allow PrimeTel to reduce its OPEX and CAPEX, since the power consumption and energy costs (a decrease of 50% in power consumption and 30% of energy cost is expected).
TE	For exploitation, it is important to participate in various standardization bodies to achieve a wide market acceptance. Examples are FiberChannel Energy Efficient (FC-EE), IEEE Energy-Efficient Ethernet standardization, InfiniBand® Trade Organisation, and Optical Internet Forum (OIF). The exploitation itself will consist of managing a portfolio of electro-optical communication products containing the adaptive technology.
TUD	• Offer of design, modelling, simulation and measurement know-how and services for broadband ICs to academic and industrial partners or other interested parties • Provide IC IPs to interested companies/foundries and project partners • Knowledge transfer to and education of students/PhDs, engineers and researches who will take leading positions in industry in future • Offer for sale of patents generated in ADDPT to interested parties • Establishing a start-up company for electro-optic circuit design where the project results of ADDAPT could be commercially offered
VIS	• Sales of vertical cavity surface emitting lasers (VCSELs) and photo-detectors chips for the adaptive IC technology. • Sales of subassemblies which consist of VCSEL chip or photo-detectors chips and the adaptive IC technology.
WUT	Improve its capabilities to conduct reliable and precise measurements of the optical transmission systems and on optical interconnects and electro-optical components like VCSELs. This will allow WUT to: • Conduct further research on these topics • Provide know-how and expertize to, and collaborate with, interested industrial and academic partners. • Train well educated researchers and engineers for the EU market • Offer patents to interested parties. • Expand the curriculum at WUT with knowledge gathered in the ADDAPT project.

Deviations: No deviations occurred

Corrective Actions: Not relevant

Outlook: Proceed as planned and build further on the exploitation plans, which will be reflected in reports D2.4, D2.5 and D2.6 deepening and updates of report D2.3.

- T2.3 Standardization issues:
  Task description: In this task the activities on standardization issues are organized. This includes:
  - Consideration of existing or planned standards and technical guidelines
  - Pursuit active standardization processes and evaluate ADDAPT transceiver suitability
  - On- going active participation in standardization actions, e.g. IEC 86B WG3, IEEE 802.3ba and FC 32G
  - Introducing the adaptivity concepts into Infiniband, Fiber Channel Energy Efficient (FC-EE) and IEEE Energy-Efficient Ethernet standardization groups for instance

  Progress and results: No work was planned yet for this activity (standardization). As a first result however, we can report that we learned that the initial idea of detecting idles in a data stream divided over multiple lanes (such as e.g. in Infiniband) is cumbersome and also energy consuming. This led us to the insight that the better implementation is in the NIC (Network Interface Card), by implementing the ADDAPT functionality here, instead of in the Active Optic Cable (AOC). IBM and/or TE will pursue this idea once enough evidence has been gathered about the viability of the concept, through their relations with relevant standardisation bodies for network protocols such as Ethernet and Infiniband.

  Deviations: No deviations occurred

  Corrective Actions: Not relevant

  Outlook: Proceed as planned, and start to develop ideas how to address ADDAPT technology in which standardization bodies.

- T2.4 Dissemination:
  Task description: This task organizes the activities for the ADDAPT project dissemination. The following activities are considered:
  - Implementation and updating of internal web page on a ".EU" domain for helping to disseminate the research results and some news about the project advancement
  - Organization of a workshop in the area towards the end of the project for efficient dissemination of results and knowledge exchange with external experts
  - Organization and authoring of joint scientific publications (journal and conference contributions)

- Organization of student colloquiums and exchanges to allow optimum dissemination of results from educational perspective into practice
- Organization and placing of press releases or public materials (e.g. leaflets, posters etc.) in media or on technical events/conferences/exhibitions
- Organization of customer events for promoting the project results and approaches
- Organizing the participation of exhibition with ADDAPT project booths
- Organization of information and knowledge transfer into scientific and technical expertise forums
- Production of "Dissemination Kit"
- Promoting the project (results) via research centers/clusters (e.g. cfAED, HAEC, CoolSilicon)

Progress and results:

1. Implementation and updating of a public web page on a ".EU" domain: The webpage has been created and launched on the domain http://www.addapt-fp7.eu. This webpage opens the research results and news about the project advancement to a broad public audience. It will be updated regularly.
2. A project fact sheet as well as a project presentation has been prepared for public audience. Both can be disseminated on various events and can also be found on the ADDAPT webpage.
3. Organization and placing of press releases:
   a. Announcement on Faculty of Electrical and Computer Engineering (03. February 2014)
   b. Announcement on TUD news webpage (31. January 2014)
   c. Article in local newspaper Dresdner Neueste Nachrichten (DNN online, 30. January 2014)
   d. Article in Dresden university journal 02/2014 (04. February 2014)
4. Brief introduction of the ADDAPT project at Symposium on Optical Interconnect in Data Centers by TE on March 19, 2014 in Berlin/Germany
5. Publication of the Dissemination plan in the report "Deliverable Report D 2.3, Plans for dissemination and exploitation of results"
6. We came to the insight, that for dissemination of the potential of the ADDAPT technology, a demonstrator does not need to be 12 lanes, as stated in DOW about the demonstrator.
   An important issue is, as mentioned under 'standardisation', to implement ADDAPT technology partly in the NIC, hence to change some standardisations. To convincingly demonstrate the potential of this technology to those standardisation committees, as less complex demonstrator implementation will suffice. The focus of this demonstrator will be on the key aspects of ADDAPT, notably:
      a. Adaptivity
         i. Fast (<20 ns) switch on/off of lanes
         ii. Fast (<1 µs) adaptivity of speed per lane
         iii. Adaptive and collaborative CDR
         iv. Adaptive voltage supply for logic
      b. Speed

i. 56 Gb/s per lane at high efficiency
ii. Near-field coupling (NFC)

Deviations: No Deviations, but gained a new insight that the Demonstrator (considered important for the dissemination) shall not be 12 lanes, but 4 lanes. The 12 lanes do not add value to the concept. This will impact the task T3.6 Design of verification platform which is led by IBM and will be performed during project months M31-M39.

Corrective Actions: No Corrective Actions

Outlook: Proceed as planned and build further on the dissemination plans, which will be reflected in reports D2.4, D2.5 and D2.6 deepening and updates of report D2.3.

2.2.2 WP3 Network analysis, system design and verification platform

Introduction and objectives of WP3

The overall system architecture is developed considering the insights from the market and standardization study done in WP2. Furthermore, a network analysis is performed which determines the data load behavior network and data center applications. This information is crucial for the implementation of the adaptivity techniques and system control methods. WP3 yields the specifications for the components and the link paths which should enable an adjustable speed from 7 to 56 Gb/s. Further key goals are performance and power adaptivity, low power consumption and a link communication distance of 10 m. A verification platform for a complete optical transceiver system consisting of 4 link paths is designed, which includes all optical and electrical devices, as well as the packaging and assembling on a PCB. The verification platform is tested and benchmarked with state-of-the-art competitive approaches. The validation includes sub-system tests as well as transmission experiments of the entire transceiver system. Leader of WP3 is IBM.

List of involved partners and assigned tasks inWP3

Table 5 WP3 involved partners

Partner	Task
IBM	WP leader, system concept, adaptivity control and data protocol, design of one link path
PTL	Network analysis, design of verification platform
WUT	Testing, measurements and benchmarking; design of verification platform
All	Contributions to system concept

Executive summary of WP3 work and results

The work on WP3 started at the beginning of the ADDAPT project. During the project period of this report, an intensive study on the system concept has been proceeded on the basis of the market and application review. Most suitable standards for the ADDAPT transceiver module seem to be Infiniband and Ethernet. Different application scenarios for a possible product implementation have been determined including AOCs for instance. The system concept consists of a 4 channel transceiver, each channel for data rates of up to 56 Gb/s, with high energy efficiency and equipped

with adaptive rapid on/off switching and speed tuning functionality for additional power savings. Contrary to the DoW, the channels have been reduced from 12 to 4 due to the lack of benefit, e.g. with regard to power consumption and chip area. Investigations showed that 4 channels are sufficient to demonstrate the capability and targets of ADDAPT and can simply be scaled to by multiples of 4 channels. For the bandwidth and power adaptivity of the transceiver a rapid switch on/off approach by detecting IDLE packets of the protocol (e.g. Infiniband) has been developed. To enable a fast locking time of the CDR and therefore a rapid synchronization of the links, the 4 lanes are divided into one master and three slave lanes. By this concept, the CDR of the master lane stays locked also in power down mode and can distribute the clock to the slave lanes where the CDRs be locked faster when the links are switched on again. For the smart adaptive tuning a change between different data rates (56-28-14-7 Gb/s) is considered. Furthermore, an intensive network analysis has been started which determines different network parameters such throughputs, data rates, power consumption, Tx and Rx powers, etc. The analysis is performed over long term of several months and gives insights on the dynamic network behavior in micro- and macro-time scale.

Detailed work progress and achievements

- T3.1 System concept:

  Task description: Based on the market study, the basic system concept and architecture for the transmitter and receiver modules will be refined. System specifications will be investigated and prepared based on extended link budget studies including simulations of the whole interconnect link. The key components including their performance targets, their adjustability regarding performance and power, as well as suited interfaces, are defined. This includes also design rules for appropriate packaging/assembling and connection/pad alignment. First conceptual analyses regarding the power saving for adaptive systems are performed taking the network data load analysis into account. Furthermore, expanded studies on the application of the higher order modulation formats in adaptable optical links and applicability of the designated electro-optical subsystems in further optical transmission areas like the metro transmission systems will be considered.

  Progress and results:

  Application scenarios

  As a result from market studies it was found that the low-power technologies of ADDAPT are best applied as an extension to standard-based optical links such as Infiniband and Ethernet. Furthermore, it was found that an important factor for the application in data center and HPC application is a rapid (i.e. <20ns) on/off functionality of the optical I/Os.

  Three possible application scenarios were identified, as shown in Figure 1:

  (a) Active optical cable replacement

  In this scenario, an active optical cable (AOC) is designed including the ADDAPT functionality. While a conventional AOC always transmit data at the maximum rate, the ADDAPT AOC reduces power consumption by implementing rapid on/off switching functionality. The data stream is analysed and the presence of active data or IDLE symbols

is detected. If the entire bus is IDLE, all lanes except a master lane are switched off. The master lane always maintains phase locking of the link bundle. If active data is detected after the IDLE sequence, the link is waked up. During wake-up time, the active data is stored in a FIFO to avoid losing data.

(b) Direct-drive optics

This case is similar to case (a) with the difference that the ADDAPT I/O is implemented on the same chip as the data generating device, which can be a processor, a network interface card (NIC), a router chip or other ASICs.

(c) ADDAPT logic integrated into the NIC

Ideally the rapid on/off control logic can be integrated into the NIC. In this scenario, the NIC tells the Tx when data is to be transmitted on the optical link, which obsoletes a FIFO to store the data during link bring-up. This scenario requires however that the link standards (e.g. Infiniband or Ethernet) include the ADDAPT functionality in its protocol, for example as an extension to already existing low-power modes such as Green Ethernet.

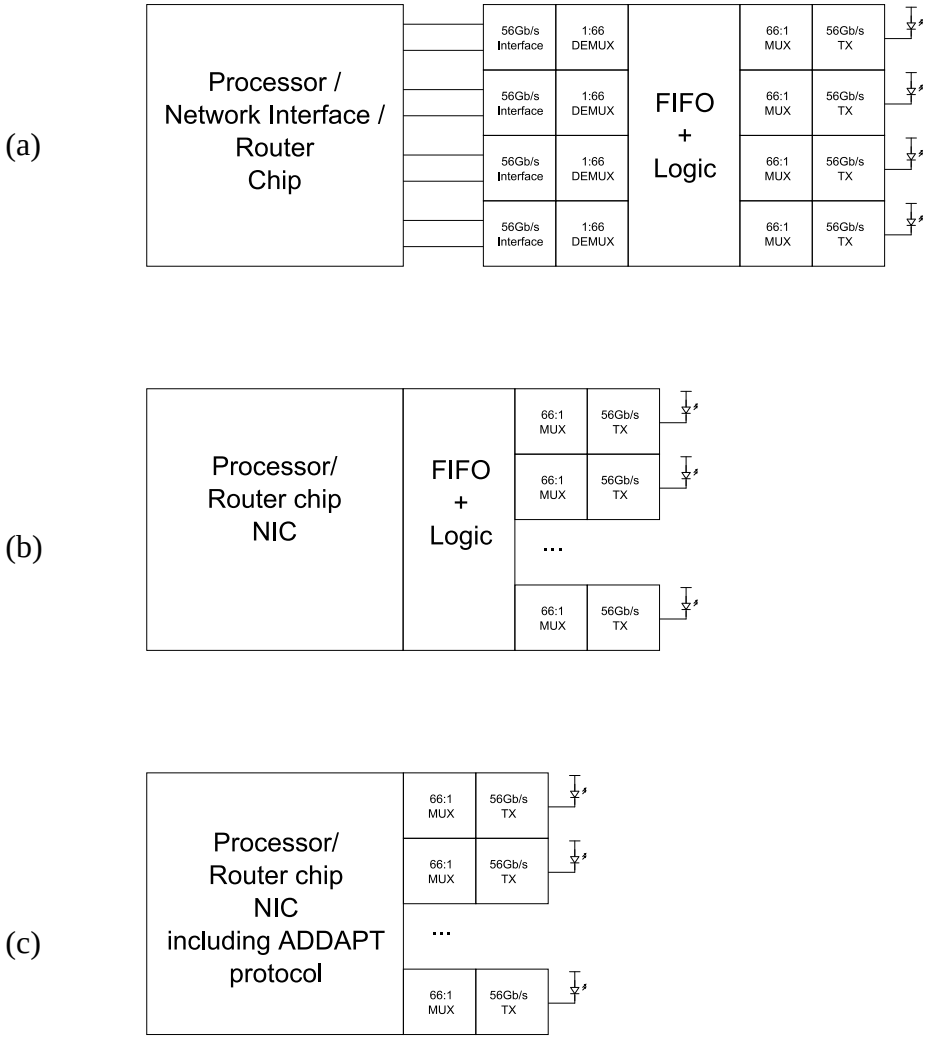


Figure 1: Application scenarios for ADDAPT

The active optical cable was chosen as primary demonstrator vehicle. The main difference to a direct-drive optics using ADDAPT is the existence of electrical links (in addition to the optical links) to provide and receive the data. The product vision is to be able to replace an existing AOC with an ADDAPT AOC to reduce the consumed power in the optical link, as shown in Figure 2.

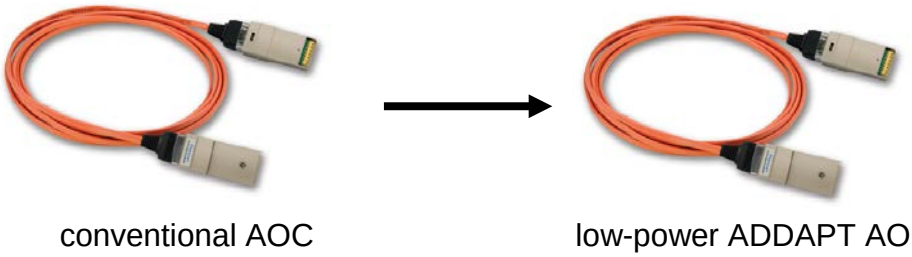


Figure 2: A low-power ADDAPT AOC replaces existing AOC to save energy costs

Envisioned implementation of AOC using ADDAPT

Figure 3 displays a block diagram of an envisioned active optical cable (AOC) product using ADDAPT technology in a 4x Infiniband configuration. As described above, there is one master lane, and three slave lanes. The master lane is always switched on, which allows the system to

- constantly maintaining phase lock, and
- have an always ready connection to transmit wake-up command to the slave lanes.

It is assumed that the phase delay over the optical connection between the master lane and the slave lane is only changing slowly, and it is sufficient to track fast phase variations only on the master lane. The timing between the master lane and the three slave lanes is adjusted only very slowly, which reduced the power for clock recovery in the slave lanes.

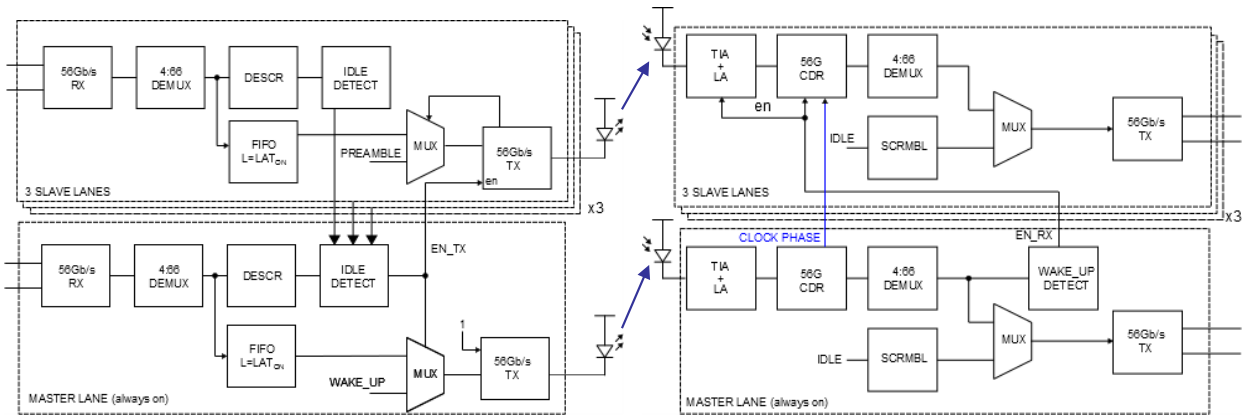


Figure 3: Envisioned Tx and Rx block diagram for 4-channel AOC product using ADDAPT technology

The data is first received from the electrical interface via 56 Gb/s electrical links, which are assumed to be always on. Switching off the electrical links as well would require to include the ADDAPT functionality in the NIC, as described in application scenario (c), which would require a modification to the existing Infiniband or Ethernet standard. The received data is demultiplexed to 1/66 rate, and fed to a digital logic block running at 1/66 the data rate, corresponding to a single 8 byte Infiniband packet using 64/66 bit coding. Also, the relatively

slow clock of the digital logic allows one to reduce the power consumption in the digital block. After descrambling, IDLES symbols are detected. If all four lanes carry only IDLE symbols the three slave lanes are switched off. Upon detection of non-IDLE symbols on one or more lanes, the slave lanes are woken up again. For this, a special wake-up symbol is sent over the master lane to the receive side, and the wake-up sequence is initiated. This means that the Rx frontend is switched on, proper bias voltages and currents are applied, and the slave CDR locks to a preamble sequence transmitted during wake-up.
At the Tx side, the data always goes through a FIFO before being transmitted. The length of the FIFO corresponds to the wake-up time of the receiver. The data can be stored unscrambled in the FIFO since the packet structure is not changed with respect to the case without the rapid on/off switching. However, since IDLEs have to be "faked" at the receive side during the time when the slave lanes are down, the IDLE generator has to use scrambling to properly insert the IDLE symbols.

ADDAPT demonstrator to capture necessary functionality for envisioned product

Since the effort to implement a product-like system as shown in Figure 3 is outside of the scope of ADDAPT, the system demonstrator shown in Figure 4 was defined, where overhead complexity was removed without scarifying the possibility of demonstrating ADDAPT functionality (i.e. 56 Gb/s optical data transmission at low power, rapid-on/off, and speed optimized settings of biases and supplies to achieve minimum power.) In this system, the IDLE detect logic and FIFO is replaced by an external pin $ACTIVE/\overline{IDLE}$, which indicates if the current data packet contains active DATA or only IDLE symbols. This signal originates from a high-speed pattern generator, where it can be programmed to mimic actual data statistics (e.g. a link with 10 % overall utilization and a given distribution of packet sizes and inter-packet delays). This will allow measuring the rapid switch on/off behaviour and power consumption under varying link statistics.

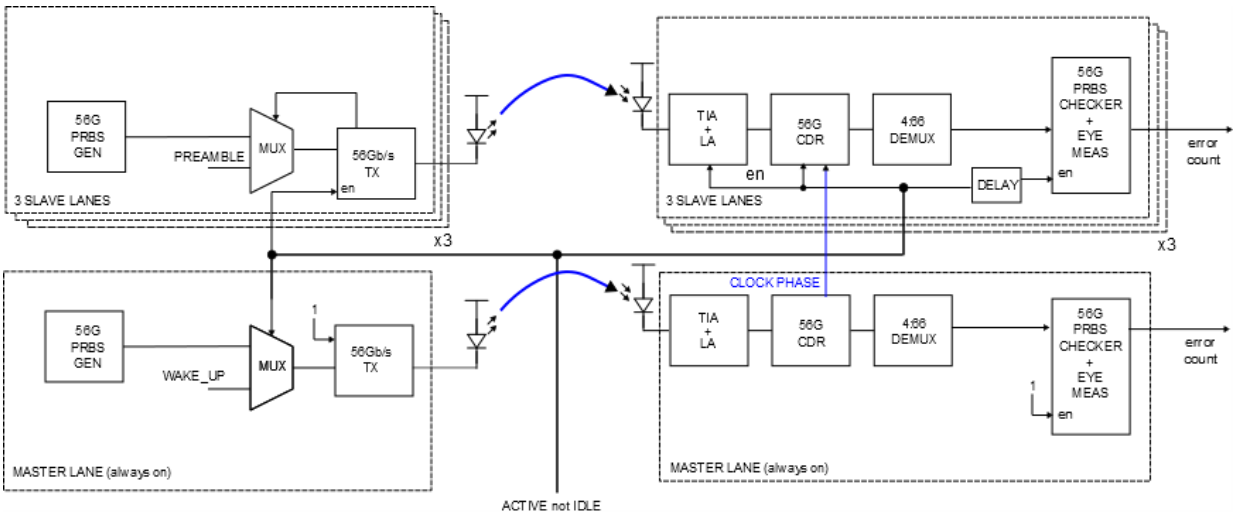


Figure 4: ADDAPT demonstrator

- T3.2 Network analysis:

  Task description: The aim of this task is to perform an intensive analysis of a real network operator's network behavior with regards to data load, performance and power consumption. The target as indicated in the DoW is to collect sufficient samples over a period of one year. Of course and where necessary data maybe captured over a much shorter time frame depending on what needs to be analysed. Different network parts will be investigated including optical core to switching and data center networks with a main objective to identify the correlation between the data traffic patterns versus the power dissipation in the various cases. From this data it will be able to identify which parts of the network consume the most energy over time, and how the energy and power consumption vary over time according to the traffic load i.e. the data throughput. This analysis will provide to the rest of the project important insights with regards to the system design and the implementation of the adaptivity approaches. The different data collected will be analysed and from these different requirements will be identified and be used for the adaptivity control design regarding the used control method, the maximum control time, latency considerations, tuning ranges etc. can be extracted. It is expected that different parts of the operator's network have different demands and hence will impose different requirements to the adaptivity approach. If one solution is to handle all it will need to be adaptive and react efficiently in all of the different cases monitored. Moreover, from the analysis it will be possible to define which components have the biggest potential to save power and there the adaptivity approach can be used most effectively. The task takes into account the future progress in optical networks with aim to provide aligned design parameters, constraints and thresholds for the design of ADDAPT's transceiver module so that it is applicable in flexible and dynamic networks. The results will be evaluated and taken into account when it comes to the design of the optical components in WP4. The complete Network Analysis study will be documented in Deliverable 3.1 which will be ready by M12 of the project.

  Progress: At the moment the task is in M9 with preliminary results already being at various links within Primetel's core optical network hence the task is still ongoing. The initial results we obtained so far come from the monitoring of two backbone links in PrimeTel's network. One was a 1 Gb/s link and the other a 10 Gb/s. Both links transferred data between an optical transport and a core switch in PrimeTel's core network. The 1 Gb/s link traffic comes from inside a city in Cyprus and the 10 Gb/s link transfers traffic between two cities in Cyprus. A high level diagram of the setup for the monitoring of these two links is show in Figure 5.
  The monitoring of the transceivers at each side of the two links was done via the Zenoss platform which is currently used for this purpose in our company. Zenoss uses SNMP requests to poll the network devices to obtain the specific measurements we require. These measurements include (a) Rx and Tx power, (b) temperature, (c) traffic load, (d) Tx bias current and (e) supply voltage. The specific optical transceivers that we monitor on these two links are on the optical transport side and are the following:

  - 10 Gb/s: MRV XFP-10GED-Sx
  - 1 Gb/s: PROLABS – GLC-S.

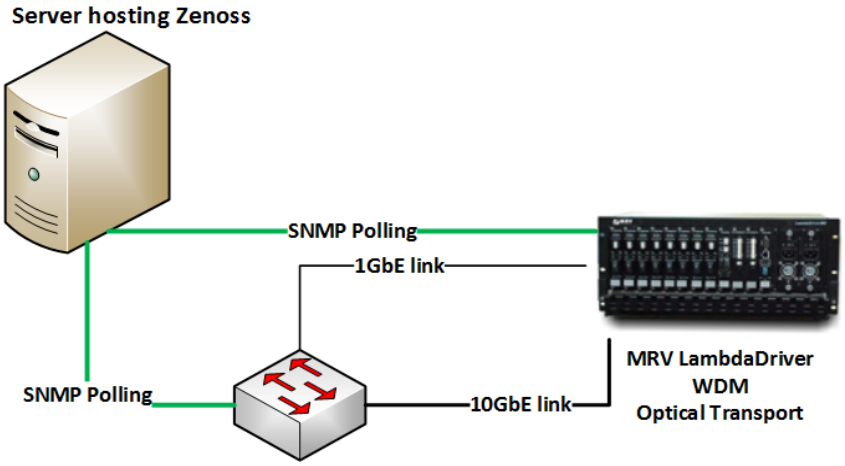


Figure 5: Initial monitoring setup

While the monitoring of the two aforementioned links is ongoing and data are continuously collected we have moved forward and started the examination of additional links that belong to the optical core of our network. These links are all high speed optical links that carry traffic between cities in Cyprus, inside a city or towards Primetel's points of presence outside of Cyprus. Moreover, specific links were chosen in an effort to identify different traffic patterns. More precisely, links that carry solely business clients' traffic are monitored in addition to links that carry traffic of normal clients were selected in order to compare their traffic patterns.

The links at this stage of the Network Analysis include both 10 Gb/s and 1 Gb/s optical links. We are currently monitoring the traffic load on these links in order to identify the most appropriate ones for our purposes. Having achieved this, we can go ahead and start measuring additional parameters as is the case we the first two links that were mentioned earlier in this document. The high level diagram of the network components we are monitoring in this stage is shown in Figure 6. Core Switch 1 and 2 refer to two core switches that are positioned in two different cities in Cyprus and the link between them constitutes one of the most important links in Primetel's network. The junction router handles traffic that is routed out of Cyprus and the Business Clients Termination Router as its name suggests is a router where solely business clients' lines terminate. On the contrary, Backbone router 1 and 2 are routers that handle traffic from normal clients. Finally, urban core switch is a switch inside the same city as Core Switch 2.

Regarding the monitoring of the link shown in Figure 6 we are monitoring specifically the traffic load. The link between Core Switch 1 and 2 is an aggregated 20 Gb/s link which includes two physical 10 Gb/s lines. Similarly, the link between Junction Router 1 and Core Switch 1 consists of two aggregate interfaces and one 10 Gb/s physical link. Moreover, the link between Core Switch 2 and Backbone Router 1 is an aggregated link that contains two 1 Gb/s physical links. This link carries normal client traffic inside a city in Cyprus. Similarly, the link between Core Switch 2 and Backbone Router 2 is a 1 Gb/s link that carries solely normal client traffic. Inside the same city is the 10 Gb/s link between Core Switch 2 and Urban Core Switch.

Finally, in our effort to identify different traffic patterns we are monitoring the link between Core Switch 1 and Business Clients Termination Router. This link carries solely traffic from business clients and the traffic patterns from our initial results suggest indeed that there is a difference in the

traffic load over time I between the traffic observed on the links that carry normal client traffic (i.e Core Switch 2 and Backbone Router 1 and 2) and this link.

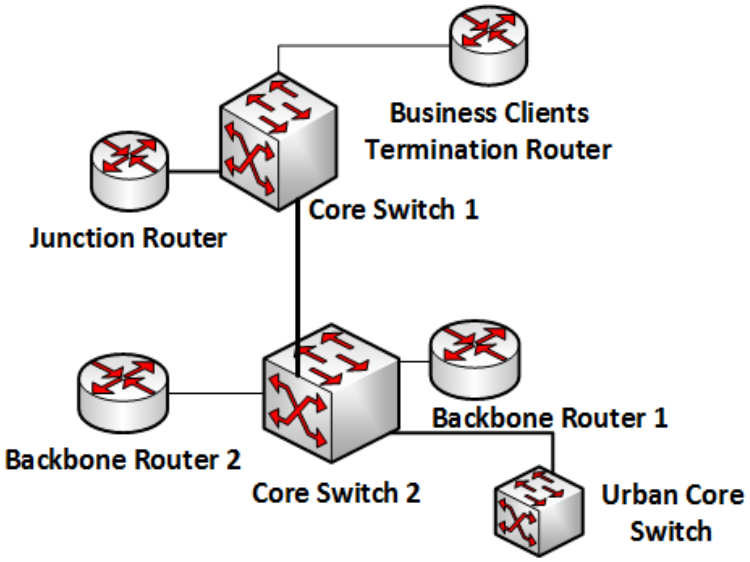


Figure 6: Current setup for Network Analysis focused on the optical core network

Results: From our initial and ongoing network analysis we have obtained some preliminary findings. The monitoring of the two links between a core switch and an optical transporter has shown that most of the examined parameters remain relatively stable or fluctuate slightly around a mean value. Namely, for the optical transceivers we monitored on these two links the temperature, Rx and Tx power, Tx bias current and supply voltage show a constant trend with minor fluctuations around a specific value. On the contrary, the traffic load that passes over those two links over the time span of one day shows as expected a wave form where each day there is a peak of traffic load from 12:00 until 00:00 of each day.

In terms of traffic load the same apply regarding the time frame of one day for the optical core links we are monitoring at this stage of the Network Analysis. In addition, we have identified a difference in traffic patterns between that of business client traffic and normal client traffic in the time span of one week. The traffic of normal clients is mostly at the same levels during weekdays with small differences in load. However, during weekends the traffic load drops considerably. On the contrary, the traffic load of business clients remains at the same levels for each day of the week.

Outlook: In addition to the ongoing network analysis we have additional plans which include:

- Monitoring the power consumption of the optical transceivers on the links we are currently analyzing.
- Include data center links in addition to optical core and backbone links.
- Expand on the identification of different traffic patterns by collecting data at dedicated links of individual customers.

➢ T3.3 Adaptivity control:

Task description: In a first step and in accordance to the market and application study as well as the network analysis, the associated data load characteristics of the required short-range optical

communication links are examined. Based on this information, different approaches for adaptivity control such as cognitive, averaged and/or real-time adaption will be studied and benchmarked. The efficiency of the smart switching and smart tuning methods will be examined and the resulting power consumption savings will be compared to standard transceivers. Appropriate algorithms are applied on top of existing or new protocols and standards. A microcontroller, DSP, FPGA or computer based control hardware is designed using look-up tables containing data load information or data load sensing devices. The control hardware must provide the optimum parameters for the optical and electrical components and link paths, e.g. number of active link paths, bandwidth per link, signal gains and amplitudes. Latency issues and advanced modulation coding schemes for performance adaptivity are considered when crucial.

Progress and results:

Basic adaptivity concepts

Two general concepts were identified to achieve power reduction by adjusting to the data volume, which are shown in Table 6. The first is rapidly switching the link on and off. The second one is dynamic speed adaptation.

Concerning rapid on/off switching, the idea is that the incoming data stream is inspected, and the link is turned off when IDLE symbols are detected. When active data is to be sent, the link wakes up. During the wake-up time the incoming data stream is stored in a FIFO in order not to lose any data. An important goal of this project is to minimize the switch-on time of the link, since it determines the required size of the FIFO, and the additional latency to wake up the link. The current goal is to keep the wake-up time below 20 ns.

Using dynamic speed adaptation allows us to reduce the power consumption of the link even further. Here, the data rates are scaled down by a constant factor (e.g. two or four). However, since power is mostly saved by reducing the supply current/voltage, which is generated by an external current/voltage regulation module, this adaptation method is several orders of magnitude slower than the rapid on/off method. The plan is to use dynamic speed adaptation at a slow timescale responding to slowly varying load patterns of the network traffic (e.g. reducing network speeds during night hours and over the week-end).

Table 6: Basic adaptivity concepts

Rapid on/off	Dynamic speed adaptation
Fast <20ns	Slow (µs – ms)
Controlled - via protocol inspection (IDLE detect) or - by NIC (requires non-standard NIC)	Controlled - by NIC depending on long-term statistics (time of day, weekday etc.)

- Rapid circuit biasing - Fast CDR locking (master / slave lane approach) - FIFO to store data while links are switched on	- All lanes run at the same rate - Highest benefit achieved by supply scaling [1] - Needs external voltage converter (slow) to get V_{DD}^2 benefit

- T3.4 Data protocol:

Task description: According to the application study performed in WP2, a data protocol will be defined, developed and implemented, which allows one to send data packets over the link while making use of the power adaptivity measures (such as number of active links/lanes, data rate, and analog parameters). The protocol shall include commands to put the link into various low-power modes and provides appropriate framing of the data to maintain data integrity. Depending on the requirements from WP2, the protocol will provide enhanced RAS (reliability, availability, serviceability), for example by employing error correction (FEC) codes and definition of spare links/lanes.

Progress and results:

Rapid on/off protocol with IDLE inspection

This section describes the data protocol which a product using ADDAPT would implement. From this we then derive the specification of a demonstrator which will allows us to verify the crucial points of the implementation (i.e. rapid on/off functionality, master/slave lanes with collaborative CDR to allow fast phase lock in freshly woken lanes).

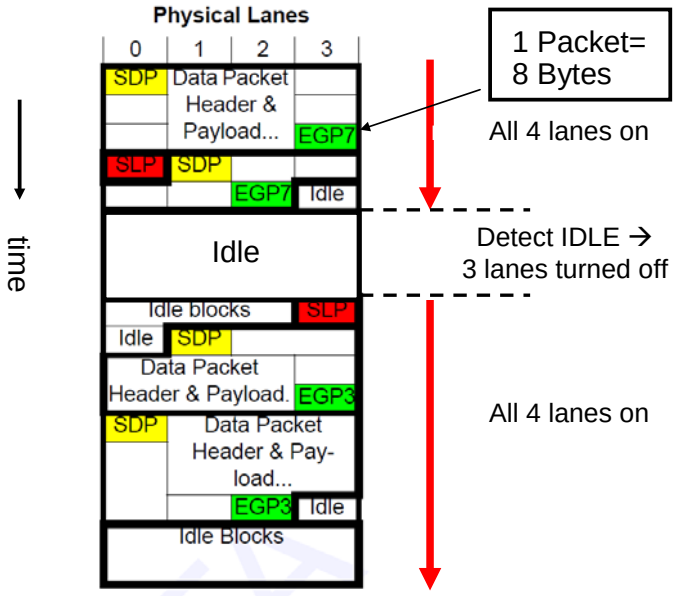


Figure 7: Data and Idle packets in a 4x Infiniband protocol

A link product using ADDAPT should avoid transmission of IDLE patterns, which in most datacentre network connections are the dominant network load [2]. This however requires that

the link needs to analyse the data sent in the cable, which in turns requires the link to understand a certain protocol. Figure 7 displays the situation for a 4x Infiniband connection. Each square corresponds to a data packet of 66 bits, which consists of 8 data bytes plus two overhead bits for clock recovery using a 64/66 code. If the IDLE pattern is detected on all lanes, all lanes are switched off except a master lane, which is always running to maintain clock synchronization.

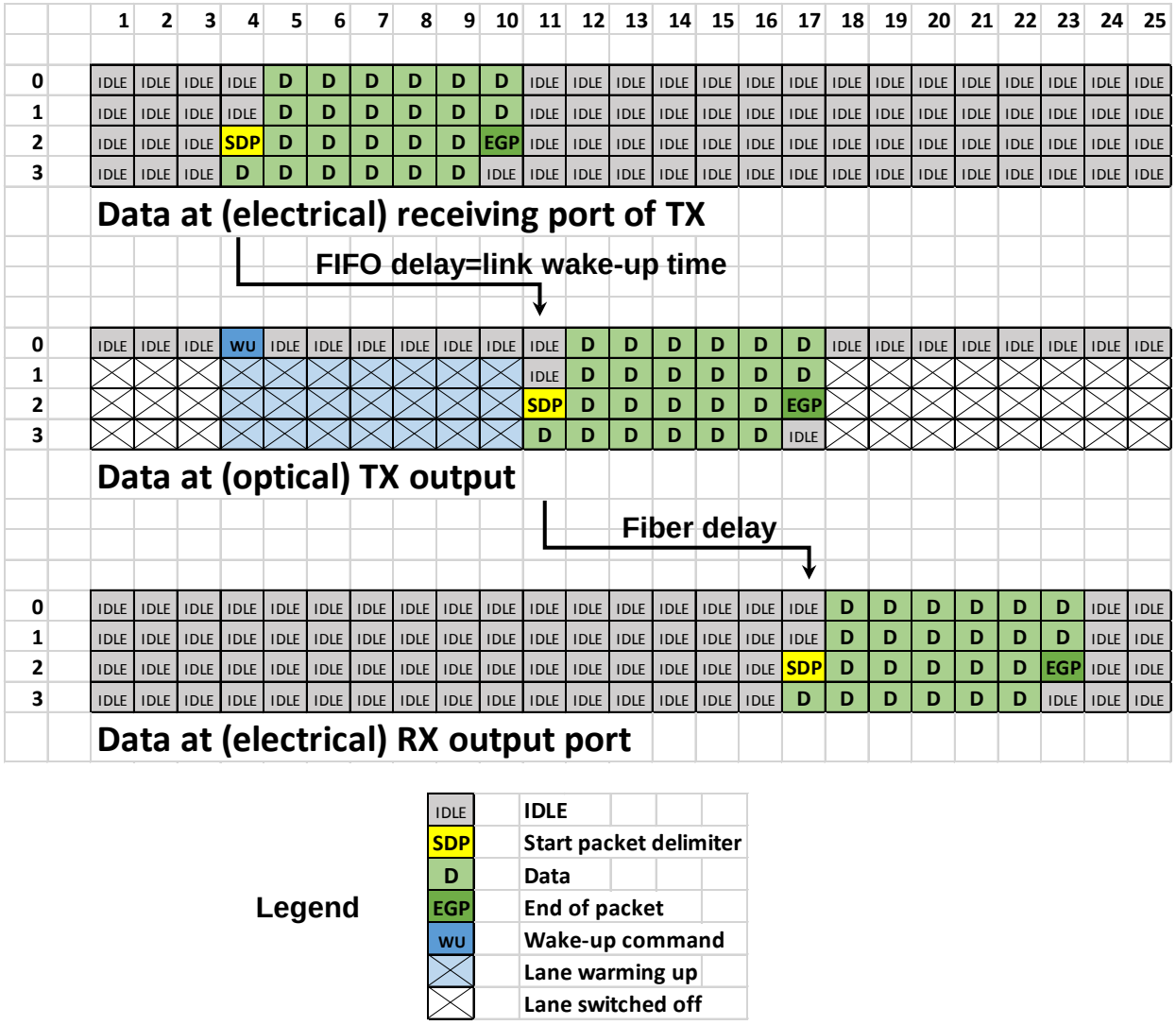


Figure 8: Data flow for an envisioned ADDAPT product using the 4x Infiniband protocol

A more detailed view of the data protocol and its switch-on/off behaviour is shown in Figure 8. The link consists of four lanes corresponding to the 4x Infiniband connection of Figure 7. The first line depicts the data sent to the optical I/Os, which e.g. is the data sent to the AOC over the electrical interface. The second line depicts the data going out on the optical link. The third line depicts the data at the electrical interface at the receiving end. Each square corresponds to an 8 Byte Infiniband packet, which is translated to 66 bits using 66/64 coding. The following packet types are distinguished, which already exist in the Infiniband standard

- IDLE: no data is transmitted
- SDP: start data packet
- EGP: end of data packet

- D: standard 8 Byte data packet

In addition, we define a new control packet

- WU: wake up,

which is sent on the master lane to tell the receiving end to wake up the three slave lanes. After reception of the wake up command, the receiver front-end and CDR circuits of the slave lanes are switched on. In order to avoid loss of data during the wake-up time, the data is stored in a FIFO at the Tx side. The required FIFO depth is proportional to the achievable wake-up time, and is given by:

$$N_{bits} = T_{wake\_up} f_{sym} ,$$

where T_{wake_up} is the wake-up time , and f_{sym} is the data rate. For example, assuming 20 ns wake-up time, and the link running at 56 Gb/s results in a required total FIFO depth of 1120 bits. The received data from the electrical interface is always stored in the FIFO, which leads to a constant penalty in latency corresponding to the wake-up time.

- T3.5 Design of one link path:

  Task description: One link path is designed to verify the functionality and interplay of the transmitter (VCSEL, LDD, etc.) and receiver (TIA, CDR, LA, etc.) components designed in WP4 and WP5, and the PCB and packaging performed in WP6. The link must be capable for adaptive transmission from 7 to 56 Gb/s and must have switch-on/off functionality.

  Progress and results: This task has not been started yet. It will start in project month M13 (November 2016) it will be performed until project month M30 (April 2016).

- T3.6 Design of verification platform:

  Task description: Based on T3.1 to T3.4, and WP6, an entire optical link system verification platform will be designed and corresponding hardware will be realized. It consists of the 4 parallel transceiver link paths with an aggregated data rate of up to 0.224 Tb/s. It is envisioned that this verification platform is compatible with PTL's data center platform to possibly test it in a real environment. This has to be evaluated during the project.

  Progress and results: This task has not been started yet. It will start in project month M31 (May 2016) it will be performed until project month M39 (January 2017).

- T3.7 Testing and benchmarking:

  Task description: The sub-systems and the full verification platform are measured in a lab environment. Optionally, the verification platform might be tested additionally in realistic environments such as PTL's data centers or optionally IBM cluster computer system, if appropriate. The following key parameters will be characterized: data rate, bandwidth, power consumption (supply voltage and current), latency, BER and device dimensions. The power savings and, if the case, drawbacks due to adaptivity are documented. Last but not least benchmarking with other optical interconnection systems will be performed.

Progress and results: This task has not been started yet. It will start in project month M28 (February 2016) it will be performed until project month M42 (April 2017).

Outlook

In the next project period the system concept will be further defined and first realizations will show its feasibility. The specification of the system and the parameters for the components will be finalized based on electrical and optical link budget consideration. System and link simulations have to be performed to gather a closer view on the power consumption models taking the adaptive features into account. Thus, the design in WP4 and WP5 can start or continue towards system requirements. The use of the data protocol for the adaptive on/off switching will be further verified and its potential for energy saving evaluated. With the design of one link path a first insight about the successful achievement of the data rates, the low power consumption and the implementation of the adaptivity approaches can be obtained. The network analysis will be continued and finally evaluated for the application of the adaptivity approaches. A deliverable report D3.1 will summarize the system concept and network analysis results and evaluation.

2.2.3 WP4 Adaptive optical components

Introduction and objectives of WP4

In this WP the low power consuming optical transceiver components and the optical coupling will be developed and evaluated. The focus on the design of VCSELs and PDs by VIS will be on power adaptivity that will be achieved by adjusting the modulation currents and modulation voltages to yield adjustable data rates from 7 up to 56 Gb/s. The use of feed forward equalization or pre/deemphasize techniques and advanced modulation coding schemes will also be considered. Exact models of the VCSEL and PD devices will have to be derived and these will be necessary for the IC design in WP5.

To obtain easy coupling and low power consumption of the entire optical transceiver, a coupling method to multimode or single-mode fibers with simple adjustment and very low losses will be necessary. Therefore, novel near field coupling will be investigated by IBM and applied to VCSEL and PD devices by AT to build NFL and maybe NFPD components. The fabrication VCSELs and PDs will be performed by CSTG based on the novel VIS designs. Multiple technology cycles (two for PDs and three for VCSELs) are planned. WP4 is led by VIS.

List of involved partners and assigned tasks inWP4

Table 7 WP4 involved partners

Partner	Task
VIS	Design of VCSEL and PDs
CSTG	Fabrication VCSELs and PDs
IBM	Design and fabrication of optical coupling elements
WUT	Testing of optical components
TUD	Modeling of VCSELs and PDs

Executive summary of WP4 work and results

First concepts and specifications for optical components were stated and discussed. The deliverable D4.1 about the concepts and specifications of optical components is submitted. It is necessary to establish a close collaboration in the development of optical components and analog electronics which include equalizing functions to reach the goal of an adaptive optical connection with speed of up to 56 Gb/s. Current optical chips are provided to the partners to derive new circuit models for the design of the analog electronics. Discussions about near field coupling (NFC) of the optical components were started but no verified concept exisits today. Close collaboration of VIS and IBM will be started in the second half of 2014 about that subject.

Detailed work progress and achievements

- T4.1 Concept and specifications for optical devices:
  Task description: In this task the specifications for the optical devices will be derived based on the insights from the market analysis and system design. Furthermore, the boundaries regarding the electrical circuits and the packaging have to be considered. The specifications give first design rules for the IC design and have significant influence of the processing of the devices.

  Progress and results: In the first project phase the basic concept of a VCSEL for the near field coupling (NFC) as well as the general concept of the optical coupling arrangement was developed for the demonstrator. Details need to be developed together with the partners AT and IBM in the framework of the project. This research includes simulations of the NFC as well as a discussion of the manufacturability of certain designs of chip devices as well as the optical coupling elements. VIS provided an estimation of some VCSEL and PD characteristics based on the experience of component designs of standard VCSEL and PD. The target of the very high speed performance of up to 56 Gb/s will be possible only in combination with special driving and fast TIA electronics with some type of equalization. Therefore, close collaboration with the analog IC development is necessary. There was submitted the first deliverable D4.1 about concepts and specifications for optical components.

- T4.2 VCSEL and NFL Design:
  Task description: In this task the VCSELs will be designed towards the specification given in T4.1. Adaptivity will be achieved by changing the laser diode current which results in an adjustable resonance frequency and therefore an adjustable bandwidth. The intrinsic trade-offs for VCSEL and NFL performance figure-of-merit (including bandwidth) and power consumption will be investigated and optimized. Since the CMOS driver ICs just provide small output signal swings at high frequencies, the VCSELs and NFLs should only require low voltages. Further goals are small VCSEL capacitances to achieve higher bandwidths and small modulations currents. Furthermore, exact equivalent circuits of the lasers have to be found in order to include the devices electrical parasitics into the IC design. Thus, intensive simulations on the lasers will be performed.

Progress and results: For the modelling and design of a VCSEL for NFC it is necessary to apply a 3D-model of a device. With such a model it is possible to model the 3D field intensities of the various modes in certain geometry and to analyse the effects of design modifications. In the first months such a 3D-modelling capability was established at VIS which will be used to develop the special VCSEL design for the NFC for ADDAPT.

- T4.3 Photodiode design:
  Task description: For power-efficiency the operation of the PD at different low bias voltages will be optimized and efficient (adaptive) biasing of the PDs via the TIA circuit will be investigated. Further design goals are low conversion losses and high responsivities. A PD model for the IC design has to be extracted from simulations and measurements.

  Progress and results: Most critical feature of the receiver is the reach of high speed response in combination with high responsivity and low dark current which can be well reached by a PIN detector. Therefore, there is selected a GaAs PIN detector with a mesa structure on a semi-isolating substrate as basic design. The active diameter of the PD should be as large as possible to reach an easy optical coupling to the device. On the other hand the diameter must be reduced to reach an acceptable bandwidth. For the first modelling phase there were provided to the project partners some small signal circuit model parameters of first high speed PDs. Further there were provided samples of PDs with various sizes for detailed evaluation of new device models. Based on these results as well as the development of concepts for the NFC there will be the final design of the PD selected for the ADDAPT project.

- T4.4 Near field coupling and waveguides:
  Task description: In this task a novel near field coupling (NFC) approach will be developed to achieve easy adjustment with minimum coupling losses between the VCSEL and PD devices and the optical waveguide. VCSELs with different apertures, cavity thickness and the DBR periodicity will be investigated to characterize their most intense excited emission modes, wavelength and corresponding tilt angels. The NFC element will be analyzed and optimized towards coupling efficiency.

  Progress and results: First discussions are started with IBM about the manufacturing technology of the coupling elements with waveguides. The basis of the coupling elements will be the technology of polymer optical waveguides which already was demonstrated by IBM. A description of that approach is included in the deliverable D4.1. Detailed work on the special design for a NFC will be started in the second half of 2014 with an additional researcher about that subject at IBM.

- T4.6 VCSEL/PD fabrication:
  Task description: In this task, the improved and optimized VCSEL and PD devices will be fabricated by CSTG in three technology cycles. Due to the advanced performance specification of those devices new high speed VCSEL chip fabrication processes have to be developed. The

new process and design will be adapted from the current CSTG sub-10 Gb/s VCSEL manufacturing process, and will be optimized to realize the final device design of VIS.

Progress and results: A continuous communication about details of the manufacturing process of VCSELs has been established between VIS and CSTG. Initial work on VCSEL fabrication at CSTG focused on the development of a new process - benzocyclobutene (BCB) deposition and patterning, which is necessary for the fabrication of high speed VCSELs. CSTG have bought and installed the equipment necessary for implementing the BCB process (spinner, oven and hotplate) and have developed process modules for depositing and patterning BCB films of the required thicknesses. In parallel with this, CSTG have completed the photolithography mask design and process flow documentation required for high speed VCSEL fabrication. VIS has supplied CSTG with high speed VCSEL epitaxial wafers of their own design and CSTG have completed test fabrications to characterize etch and oxidation processes. The first full VCSEL process fabrication iteration has started and it is expected that prototype devices from this effort will be available in the second half of 2014.

- T4.7 Testing and benchmarking of the optical components:
  Task description: First on-wafer tests of the VCSEL and PD devices will verify the general functionality of the components. Afterwards, the individual and coupled components and subassemblies will be characterized by static and high-frequency measurements by WUT. By adjusting separately characterized bias current and other operating parameters, the trade-offs between performance and power consumption will be determined. On this basis the components will be optimized and redesigned.

  Progress and results: WUT established a full setup for HF-transmission measurements up to 56 Gb/s for one transmission channel and carried out tests of complete packaged optical communication modules. The measurement setup for bare optical chips is in development. VIS provided WUT a first set of standard bare VCSEL and PD chips for first tests. Proposals for the testing of the final demonstrator with 4 channels have to be discussed in detail with the project partners.

Outlook

Detailed modelling of new designs of optical components based on the discussed and derived concepts will be performed in the next project phase. Circuit model parameters will be derived for existing optical components and will be used for the design of the analog electronic circuits. The discussion and modelling of special NFC solutions will create a brighter view on the opportunities to reach a simplified optical coupling for the assembly of the components. The influence of the various parameters of the components and coupling scenarios to the overall optical power budget of the transmission will be analysed and the appropriate solution will be selected as basis for the production of the components for the project demonstrator.

2.2.4 WP5 Adaptive integrated circuits

Introduction and objectives of WP5

High-speed electrical transceiver circuits are the main system components which are able to react flexibly on varying bitrates of dynamic networks. The optical devices are primary steered by the ICs, thus depending on their adaptivity capabilities. Moreover, electrical ICs consume lots of power. Therefore, special focus is given on the power-efficient design and on adaptivity enabled by novel circuit concepts. This includes especially the development of LDD (optionally including level and power control circuits), TIA, LA and CDR circuits. If the transceiver system is dedicated for standards or applications dealing with sub-data rates optionally multiplexer, demultiplexer and frequency divider circuits are implemented. Power and performance adaptivity is applied by changing the bias current, the clock frequency and if fruitful the bias voltage. In addition, a rapid switch on/off capability will be implemented to turn off the links when no data will be transmitted. Furthermore, the use of pre-/de-emphasis and equalization techniques or advanced modulation coding schemes is considered to achieve high data rates together with the optical components. The design of the electrical transceiver ICs will be realized in very advanced 14 nm IBM CMOS technology and optional in 28 nm CMOS technology from Globalfoundries. An adjustable data rate from 7 up to 56 Gb/s is targeted. Successful IC design requires the knowledge of exact models of the optical components and their connections to the ICs. Bandwidth peaking techniques such as inductive series peaking, inductive load peaking, transformer coupled peaking and emitter generation with parallel RC elements will be considered to further relax the speed-to-power consumption trade-offs. WP5 is coordinated by TUD.

List of involved partners and assigned tasks inWP5

Table 8 WP5 involved partners

Partner	Task
TUD	WP leader, transmitter IC design (LDD, MUX, pre-emphasis/equalization), receiver IC design (TIA/LA), IC test and measurements
IBM	Receiver IC design (CDR), digital logic design
WUT	IC/sub-component test and measurement
All	IC and sub-component specification

Executive summary of WP5 work and results

In the reported project period the initial concepts and specifications for the adaptive transceiver ICs have been derived from different requirements which include potential markets and applications, the system concept, the optical components and the assembling/packaging techniques. A high data rate of up to 56 Gb/s and a high overall energy efficiency of around 4 pJ/bit is targeted for the LDD, TIA/LA and CDR. Adaptivity in terms of on/off switching and bandwidth/power scaling is implemented into the circuits. The main challenge for the LDD is to enable high data rates in combination with a lower bandwidth VCSEL by using equalization technique. Therefore, a VCSEL model development is in progress. The TIA at the receiver side has to deal with very weak input currents and should therefore have a high sensitivity and low noise. The key functionality of the CDR is the rapid on/off switching below 20 ns. The realization of the different IC concepts and the

design has been already started and are in an early state. A first tape-out and fabrication of the chips is planned at the end of 2014 containing a one lane transceiver sub-system for the verification of the high speed, low power consumption and rapid on/off switching functionality.

Detailed work progress and achievements

- T5.1 Concepts and specifications for integrated circuits:
  Task description: Based on the insights from the market and application analysis and from system design, the specifications for the ICs are derived. Here, also the boundaries regarding the optical devices and the packaging are considered.

  Progress and results: Based on the market, application, on literature studies and on the system architecture discussions, the initial concepts and specification for the transceiver ICs, i.e. for LDD, TIA/LA and the CDR, are determined and investigated. A more detailed report of the progress and results of this task are presented in the deliverable report D5.1 'Specifications for adaptive transceiver ICs' which has been delivered in August 2014.
  The ICs will be designed in a 14 nm CMOS technology of IBM. For this, a circuit design environment has been established, for which the involved researchers form TUD got access and were trained in the design and layout techniques. Afterwards, some standard TIA and LDD circuits were designed as trials to get confirm with the technology and estimate its performance and reliability. In addition to the 14 nm technology, additional IC design in a 28 nm CMOS technology from Globalfoundries is planned where TUD has access to. The circuits in this technology are used to investigate and evaluate different bandwidth peaking techniques to achieve high bandwidth and adaptivity approaches to reduce the power consumption.
  From the market, application and standardization studies in WP2 it has been figured out that in the near future single channel data rates of more than 50 Gb/s are required. For example in Infiniband the HDR and NDR requests 50 Gb/s and 100 Gb/s, respectively. For Ethernet it is expected that that the servers have to provide 100-Gigabit Ethernet in 2017. Therefore, an increase of the transceiver channel data rates is mandatory and for the ADDAPT ICs a data rate of up to 56 Gb/s is targeted. At the same time, the aim of network, data center and high performance computing operators is to lower the power consumption of the systems in order to save energy, lower the heat dissipation and therefore the cooling efforts and last but not least to reduce the operating costs significantly. Thus, the power consumption of the ICs have to be lowered which can be achieved by using advanced and highly scaled technologies with inherent low power consumption, like 14 nm CMOS leading to high energy efficiency. Furthermore, the optical links with static performance of today have to become variable and dynamic in future with regard to changing demands and conditions in the network. Performance and power adaptivity in the links enabled by adaptive circuits will be one solution to achieve an additional energy saving. This needs to equip the ICs with capabilities for a rapid on/off switching and tuning of their bandwidth and power consumption. The tuning can be achieved by changing the circuits operating point, e.g. the bias currents (and voltages). If lower data rates are sufficient, the supply current can be reduced and power can be saved. At the same time, the transit frequency and transconductance of the transistors is reduced. Therefore, the bandwidth and

noise of the amplifier is decreased. Unfortunately, this also leads to a drop of the amplification which has to be compensated since usually the output levels are required to be constant. This can be achieved by adjusting the load impedances for instance. Preliminary simulations on standard TIA and LDD circuits revealed that a reduction of the bandwidth by 50 to 70 % the power consumption can be reduced by at least 50 %.

From the technical point of view the design of the ICs is strongly connected to other technical aspects such as the system concept, optical components and the assembling and packaging. General system aspects include a low supply noise to keep the jitter extremely small for the high speed signals. Since the final transceiver contains 4 lanes, IC arrays are used. Thus, cross-talk can occur e.g. via power and ground wires which has to be carefully considered during the design phase. From initial studies on the optical components it has been figured out that for the vertical-cavity surface-emitting lasers (VCSEL) it will be difficult to achieve a data rate of 56 Gb/s by themselves due to physical limits. Thus, the LDD has to provide a proper pre-emphasis or equalization technique to overcome the bandwidth bottleneck of the VCSELs. This needs the development of a precise VCSEL model and co-simulations of the LDD and VCSEL. Currently, a nonlinear VCSEL model based on rate equations is realized. Furthermore, the LDD has to provide sufficient bias as well as modulation voltages and currents to the laser. On Rx side the TIA has to deal with very weak photocurrents due to low optical received powers. From the optical link budget it is expected that the optical OMA power at the receiver is between -12 dBm and -9 dBm. Thus, the TIA should have a high sensitivity for photocurrent amplitudes between 16 and 31 µA. At the same time the transimpedance gain should be high and in the order of 10 kΩ. The TIA input referred noise should be minimal and show a maximum value of 4 µA. Regarding assembling and packaging, the ICs are required to enable wirebond connections which have to be taken into account for pad sizes, positions and pitches. Especially, the pad sizes will have a significant impact on the performance of the ICs due to parasitic capacities. The bondwire connection has to be considered and involved into the IC design as well due to parasitic inductances. The concepts and specification of the optical components and the packaging and assembling techniques, which have influence on the IC design, are explained in more detail in the deliverable reports D4.1 and D6.1 which are already available. A report D3.1 on the details of the system concept and architecture will be available by October 2014.

The state of the art of the main transceiver ICs has been reviewed. Adaptivity concepts where the bandwidth and power consumption is scaled in the circuits is only rudimental existing. Only one work was found for a low data rate optical link system where the bandwidth was scaled by tuning the supply voltage. For LDDs data rates up to 40 Gb/s were only achieved in BiCMOS showing energy efficiencies above 2 pJ/bit. Circuits with pre-emphasis or equalization for the VCSEL show data rates up to 64 Gb/s, but with a power consumption of 900 mW resulting in a high energy per bit of 14 pJ/bit. The LDD of ADDAPT including equalization is expected to have an energy efficiency of approximately 1 pJ/bit at 56 Gb/s. TIA circuits for data rates up to 40 and 50 Gb/s has been implemented in BiCMOS and CMOS technology with average energy efficiencies of 1 pJ/bit or below. For the ADDAPT TIA including a LA an energy per bit of 0.7 pJ/bit is estimated at 56 Gb/s. CDRs are commonly designed in CMOS technologies and can achieve 40 Gb/s with power consumption below 100 mW resulting in energy efficiencies of around 2.5 pJ/bit which is in the order of the ADDAPT designs. However, the ADDAPT CDR

will be equipped with adaptive functionality. In Table 9, Table 10 and Table 11 the current main specifications of the LDD, TIA/LA and CDR circuits are shown for one link path.

Table 9: Summary of targeted VCSEL driver specifications.

Parameter	Min	Max	Unit	Remarks
Bias current	0.3	8	mA	
Modulation current	4	8	mA	
Supply voltage (driver)	2.5	3	V	
Supply voltage (digital)	0.8	1.2	V	
Power	tbd	60	mW	Adaptive
Bit rate	7	56	Gb/s	Adaptive
Turn-on time	tbd	10	ns	

Table 10: Target parameters of the analog receiver front-end.

Parameter	Target value	Unit	Comment
Bandwidth	20 (with DFE) 28 (without DFE)	GHz	To be determined by system simulations of the DFE
Transimpedance gain	8-10 (78-80)	kΩ (dBΩ)	
Power consumption	28	mW	Soft target

Table 11: CDR Specification for one link path.

Parameter	Value	Unit
Data rate	56 – 28 – 14 - 7	Gb/s
Energy efficiency @ 56 Gb/s	2.5	mW/(Gb/s)
Lock time	10	ns
Input signal level	100-150	mV
Common mode range	650-750	mV
Frequency offset	±100	ppm

Three IC design runs in 14 nm CMOS are planned with one approximately every 12 months. In the first iteration step single initial high-speed designs are developed to achieve for the first time 56 Gb/s circuits with lowest power consumption. Simultaneously, these designs are used to verify the models of the optical components and the CMOS technology as well as its process variations. Pre-/deemphasize and equalization technologies will be used to relax the bandwidth requirements of the ICs and the optical components. This first IC run is planned to take place by the end of 2014 and will be used to implement a one lane subsystem which will be used for the verification of the speed, low power consumption and the rapid on/off switching of the link. On this basis the circuits will be further optimized in the second run and equipped with the adaptive tuning concepts. In the third run, the four lanes Tx and Rx system will be integrated on one chip. During fabrication of the 14 nm chips, 28 nm will be used for additional tape-outs of single ICs.

- T5.2 Transmitter IC design:

  Task description: Transmitter design includes the LDD (optionally including level and power control as well as multiplexer with retimer and frequency divider). Power and performance adaptivity is studied by means of controlling the bias points of the circuits. Priority is given to current/voltage control and on/off switching. For bias voltage control dc/dc converters or regulators will be used. Targeted adjustable output voltages and currents for optimal driving of the VCSELs are in the range of 2 V and 5 mA at a maximum data rate of 56 Gb/s. Reduction of the modulation voltage (or current) in the low data rate mode is investigated. To achieve high bandwidth, different bandwidth enhancement techniques such as positive feedback, pre-emphasis, equalizing filters and hybrid or inductive peaking for instance will be evaluated.

  Progress and results: The transmitter design has recently been started in project month M05 (May 2014) and is at a beginning state. From the concepts phase and also referred to WP4 it figured out that the data rate of 56 Gb/s can only be achieved by implementing pre-emphasis or equalization into the LDD to overcome the bandwidth bottleneck of the VCSELs. To achieve this, the VCSEL characteristic and parasitics have to be taken into account for the design. Therefore, an intensive modelling of an existing 40 Gb/s VCSEL from VIS has been performed and a derivation of a nonlinear model based on rate equations is in progress. From this model it will be possible to determine the trade-off between the equalization (e.g. number of taps) and power consumption to find the optimal modulation point. Another challenge is the low power design and at the same time tuning the driver power versus link speed. The supply voltage of recent submicron technologies is below 1 V. Therefore. all the digital sections, the pre-driver, and equalizer would use this supply voltage. However, the laser on-state voltage is around 2 V and so there is a need for a higher supply voltage for the driver stage. Therefore, two voltage domains are defined: 0.9 V (VDD_1) and 2.5 V to 3 V (VDD_2) which have to be provided.

- T5.3 Receiver IC design:

  Task description: The receiver design includes the TIA plus LA (developed by TUD), and the CDR circuit (developed by IBM). Optional demultiplexer may be required. Speed/power adaptivity and on/off switching concepts are considered for these circuits as well. Controllable current and voltage sources are applied to adjust biasing and to scale power consumption with bandwidth. Also here, bandwidth peaking techniques are applied. In the receiver circuits, the noise has to be minimized. For low data rates, the decreased bandwidth coming with the adaptivity control is beneficial to reduce the dominating thermal noise.

  Progress and results: Also the receiver design has recently been started in project month M05 (May 2014) and is at a beginning state.

  The receiver amplifier consists of a TIA stage to transfer the photocurrent into an amplified voltage, multiple voltage amplifier stages to add more gain and a LA stage to stabilize the output signal level. In order to achieve a higher input sensitivity and lower noise for the TIA a reduced bandwidth-to-data-rate-ratio of 0.5 is considered. Normally, a ratio of 0.7 is used leading to a lower ISI. Therefore, in the ADDAPT TIA a one tap equalization (DFE) is included and a higher ISI can be accepted. This is a quite new concept which can lower the requirements

for the TIA input. For the TIA design, a resistive feedback inverter has been chosen. This topology possesses an excellent compatibility with the technology. It is based on a standard digital inverter, with feedback resistor between the input and the output node. A differential pair structure has been chosen for the voltage amplification chain. To maintain the bandwidth, inductive peaking has been used to boost the bandwidth of the amplifier. In the final design, the inductance will be realized using active inductors instead of peaking coils in order to conserve chip area. The amplifier chain is terminated by a voltage limiting stage. This stage is also based on the differential amplifier topology. The bias current is however strongly reduced, in order to reach saturation for input peak values. Two types of adaptivity are implemented into the Rx amplifier: fast on-/off-switching and bandwidth adjustment. Fast on-/off-switching can be achieved by simply pushing the photodiode output below inverter threshold. Thus, the n-MOS of the inverter is switched-off resulting in negligible power dissipation. The differential amplifiers can be switched off by controlling their biasing current source. The bandwidth adjustment of the inverter-based TIA can be achieved by using an external voltage regulator to adjust the supply voltage or by extending the inverter into a cascode inverter and use the bias voltage for the adaptivity control. In the differential and LAs, the current sources can be modified by simple DAC structures. So far, a TIA, differential amplifier and limiting stage have been designed for operation at 25 GHz. This will be extended for higher bandwidths and for the adaptive functionalities.

For the CDR design a dual loop architecture was chosen consisting of three functional sections: a frequency synthesizer, a phase rotator (PR) and CDR loop filter. The frequency synthesizer generates the target clock frequency. A digitally programmed PR then finds the optimal sampling position interpolating among a set of discrete phases. Finally, the PR block is driven by a digital CDR loop filter and needs to align both the phase and frequency of the incoming data. The CDR circuit uses a four-phase design where each slice operates at quarter rate. This allows clocking the Rx with four quadrature phases at ¼ of the data rate, thereby relaxing the requirements of the sampling latches and the clock distribution circuits. Moreover, spreading the current among four slices makes it easier to fulfil electromigration requirements. The CDR can be powered on/off by means of an external trigger signal which shuts down the bias currents. By reducing the supply voltage of CMOS circuits, speed throttling to different data rates (56, 28, 14, 7 Gb/s) is considered as a secondary power saving approach.

- T5.4 Tests and benchmarking of integrated circuits:

  Task description: After fabrication, the circuits are verified and evaluated with respect to their performance by measurements. Small- and large-signal measurements are performed to analyze gain, matching and power consumption over frequency range. Eye-diagrams and openings are studied. Based on these insights, the device models and the analysis method are refined and the circuits are optimized and redesigned. The obtained results are compared with the state of the art. Improvements in assembling, packaging and arrangement are analyzed.

  Progress and results: This task has not been started yet. It is planned to start in project month M13 (November 2014) but will probably be delayed until the first ICs are available for testing after fabrication. However, the required measurements procedures and test scenarios will

already be examined during chip fabrication. The task will be performed until project month M36 (October 2016).

Outlook

For the chip fabrication in 14 nm IBM CMOS technology there are three wafer runs scheduled. The first run is for evaluating in the one lane Tx/Rx configuration if the high data rate of 56 Gb/s and the low power consumption can be achieved as well as for testing and evaluating the rapid on/off functionality. This run is planned to take place by the end of 2014. Thus, the first designs will be finished in few months. Besides the one lane Tx/Rx configuration also break out chips of the TIA/LA and LDD will be fabricated. A second 14 nm run is followed probably in the second half of 2015 with optimized circuits and subsystem including the IDLE protocol detection and adaptive tuning mechanisms. In a final third 14 nm run the 4 lane system will be fabricated with the full ADDAPT functionality. During the fabrication of the 14 nm implementations additional designs and wafer runs in a 28 nm CMOS technology of Globalfoundries are planned. These designs are used for investigating and evaluating different approaches for the performance and power adaptivity implementation separately. After the fabrication of the first designs, the ICs and the one lane subsystem will be verified and measured in the lab. On the progress and results of the first IC designs will be reported in the deliverable report D5.2 scheduled in project month M21 (July 2015).

2.2.5 WP6 PCB and packaging

Introduction and objectives of WP6

In WP6 the optical and electrical components developed by the partners will be packaged and assembled to form the entire system. Thereby, the main focus is to maintain the capability of the system for transmission at adjustable data rates up to 56 Gb/s during the packaging and connection process. The coupling losses between the components should be low regarding power consumption reduction. Additionally, the electrical and optical crosstalk has to be taken into account because the single dies will be closely located. In a first step, the interfaces between the components, the system and the outside world are defined. This requires close cooperation with WP4 and WP5 where exact RF models of the interfaces and pad configurations are developed to reach a proper mechanical and electrical interconnection. In a second step, the requirements for the integration and suitable packaging techniques are evaluated. Wire-bonding techniques as well as flip-chip techniques are investigated. While flip-chip offers better performance for high-speed data transmission, wire-bonding is preferred regarding space for adjustment of the optical near field coupling element. Furthermore, the appropriateness of different packaging substrates, e.g. ceramics, glass is investigated. For connection of the NFC element to the optical components an appropriate alignment and attachment technique is developed. Finally, the packaging is preceded and the system housed inside a standard transmitter case for instance. For this, proper electrical/optical interface specification of the transceiver for testing of the components and transmission is necessary. Leader of this work package is AT who develops and conducts the packaging concepts. TE will be contributing as mentoring partner due to its outstanding experience in this field.

List of involved partners and assigned tasks inWP6

Table 12 WP6 involved partners

Partner	Task
VIS	Opto-electrical chips (VCELS and PD arrays)
TUD/IBM	ICs: LDD, TIA and CDR; additional digital circuitry
IBM	Waveguide for NFC
WUT/TUD	High Frequency testing
TE	Commercialization

Executive summary of WP6 work and results

The activities stated for in Description of Work (DoW) and related to WP6 has been on schedule referring to work map.

The electrical interface has been concluded to be based on coaxial connectors in early stage of the project. There other options to utilize any pluggable interfaces are under investigation which will enable data transfer at 56 Gb/s at least for 4 lanes in parallel. This should be met for the Infiniband HDR standard which has been under development.

The HF design of demonstrator board/package has been heading to the end of its first iteration. The preliminary 3D FEM simulation results show the complete line insertion loss below 3dB (IC pad interface to coaxial connector interface). This critical design phase of demonstrator board/package will investigate several packaging approaches and its dependences to HF signal transfer. There will be also done the comparisons of simulated results versus measurements on real package.

The optical link specification has been under definition in terms of optical budget and all related parameters. This point become critical since especially optical budget has a low margin. There are several actions planned which should lead to increase the margin of optical budget. There are involved nearly all partners in this task since optical budget depends on optical packaging, optical chips (VCSEL and PD) and finally on ICs. There is also a relation to near field coupling which will be investigated together with partners VIS and IBM.

Detailed work progress and achievements

- T6.1 Packaging concept and interface definition:

  Task description: Based on the system architecture for sub-systems and the verification platform defined in WP3, the specifications for the packaging and connections are evaluated. This includes all interfaces, the used materials and geometries of the components, as well as specific properties such as signal type (high/low power, high/low frequency, etc.) and number of terminals. It has to be clarified how and on which material (e.g. glass or ceramic) an optimal low loss connection between components as well as to ICs from the outside can be achieved. The properties of all interconnections between ICs, optical chips and waveguides have to be defined. This will be the basis to start with the packaging design and the assembly concept of the transceiver.

Progress and results: There has been concluded together with consortium (all partners) the way how to test parallel data transfer via multiple 56 Gb/s links. It will be tested on so called demonstrator which has been more detailed described in deliverable D6.1. The demonstrator will be connected to outside system via coaxial connectors which can support the bandwidth up to 70 GHz. The demonstrator is shown in the following picture.

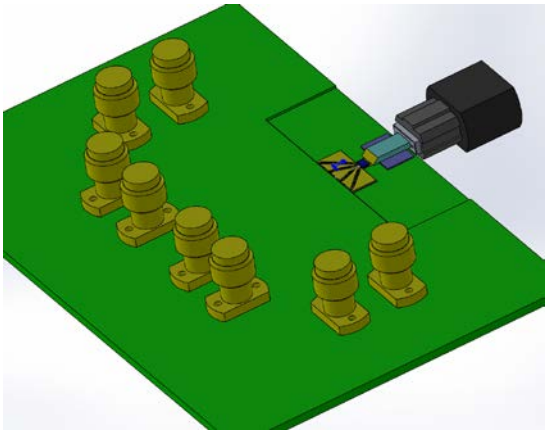


Figure 9: Packaging concept of the system demonstrator

There has already been concluded (TUD, IBM, AT) the general pad layout on ICs which will be connected to demonstrator boards. The demonstrator concept has been designing upon 3D FEM simulations. Based on preliminary results it will be done as a hybrid based on two basic boards PCB and ceramics.

Deviations: There have not occurred any deviations so far.

- T6.2 Packaging technique development:

Task description: Successful wire-bonding technique for 40 Gb/s short-range transmissions has already been shown. Depending on the IC and pad geometries and electrical properties as well as on the length of the bond wires, this technique may also be capable for higher data rates. Although this is a big challenge, side-by-side component placement and wire-bonding benefit the adjustment of the optical near field coupling element to the optical components. Nevertheless, it can influence the NFC capability due to the bonding close to the aperture. Furthermore, the wire bonding process will be limited and have a strong impact on the optical chip layout design since the pad sizes might be small there. Therefore, limits and performance of wire-bonding for high data transmission will be investigated within ADDAPT. A wedge-wedge bonding of ICs buried within a hybrid 3D substrate is investigated. As second option, flip-chip packaging by soldering of the optics and electronics on a common substrate is analyzed. This results in very short connection distances showing a good RF performance but requires the development of an optimal signal routing to connect the different components. Furthermore, it has to be taken into account that the flip-chip assembling complicates the optical near field coupling and that the heat dissipation from ICs to optical components has to be carefully considered for the design. Generally, the most promising bonding technique will be evaluated regarding RF requirements and narrow pitch applicability. Another important issue will be the consideration of electrical and optical crosstalk. Based on near field coupling, simple

1-axis alignment and adjustment of the coupling element will be studied. During this task all methods will be analyzed, optimized and compared to choose proper techniques for final packaging in T6.3. The technical development will be conducted by AT while TE supports this task with its competencies and knowledge in the packaging filed.

Progress and results: There have been investigated two basic packaging techniques the face down attach (also known as a flip chip) and face up attach (based on wire bonding). Assuming the preliminary results of HF simulation and also other aspects like optical coupling based on NFC then the final packaging approach will be based on both techniques face down and face up attach. These techniques have been described more detailed in deliverable D6.1.
The alignment work station has been under preparation for parallel optics alignment and will be controlled via PC and customized control SW.

Deviations: There have not occurred any deviations so far.

- T6.3 Component/system packaging/assembling:
  Task description: Based on the insights of T6.1 and T6.2 the best suited connection and packaging techniques will be used to combine all components for the transceiver links and the verification platform developed in T3.5 and T3.6. This also includes the adjustment of near field coupling waveguide components (developed by IBM, T4.4) to the VCSELs and PDs.

  Progress and results: The physical packaging will be started once the components will be available. There will be tested demonstrator boards excluding active components first in order to verify its bandwidth capability. This task will be done together with WUT and TUD.
  Then after proven of feasible bandwidth capabilities of packaging techniques and demonstrator itself the demonstrator boards will be packaged together with active chips and verified overall performance. Also the optical coupling methods including near field coupling will be verified. This task will be done together with TUD, WUT, VIS and IBM.
  There has not been don any particular activity so far in this point.

Outlook

The demonstrator boards HF design phase is in advanced stage and there will follow physical test of partial components including assumed packaging techniques.

2.3 *Project management during the period*

Introduction and objectives of WP1

The key objectives of WP1 are coordination and management of a multidisciplinary team of eight participating institutions, quality control, progress monitoring, reporting and communication with EC. The aim is to create a sustainable competence network in the high-speed energy-efficient adaptive optical transceiver area, which holds well beyond project end. Leader of WP1 is TUD.

List of involved partners and assigned tasks inWP1

Table 13 WP1 involved partners

Partner	Task
TUD	Overall coordination and project management
All	Reporting

Executive summary of WP1 work and results

Within the ADDAPT project coordination the contractual issues regarding the Grant and Consortiums Agreements have been successfully finished. The pre-financing of the project has been distributed and transferred to the partners. The project is established and appropriate communication between the partners is arranged. The kick-off meeting and the second project meeting were organized. Furthermore, webconferences with all or just few project partners on a regular basis are scheduled and performed. A webpage is created and updated periodically to inform and promote the public about the project. A secured data sharing system is created which can be used to exchange information and documents among the ADDAPT partners. During the reported project period, 7 project deliverables with reports have been prepared and submitted.

Detailed work progress and achievements

- T1.1 Coordination:

  Task description: The project coordination and management involves the following tasks.

  - Overall administration
  - Communication with EC, responsibility to meet demands of EC
  - Streamlining of communication, knowledge transfer
  - Continuous collaboration with the WP leaders and all researchers;
  - Strategy and practical R&D management of the project
  - Ensuring accomplishment of the technical and business objectives, Quality management and monitoring compliance by the consortium participants with their obligations, verifiable assessment and reviewing of the project against the deliverables and milestones
  - Risk management
  - Collecting, reviewing and submitting technical and financial reports and other deliverables (including financial statements and related certification) to the EC, budgeting
  - Preparing of steering board meetings, chairing meetings, preparing minutes of meetings and monitoring implementation of decisions taken at meetings
  - Coordination of external communication, participation of ADDAPT participants in public-addressed events to strengthen international and European visibility of ADDAPT research
  - Contractual management of ADDAPT (negotiation and handling of contract amendments)
  - Legal management of ADDAPT (consortium agreement, support in IPR issues)
  - Participating in activities or workshops where ADDAPT consortium should be represented
  - Design of an attractive ADDAPT logo as means of cooperate identity for enhanced recognition value of the project
  - Organization of consortium agreement

Progress and results:

Consortium management tasks and achievements

After the negotiation meeting on August 13, 2013 the GPF documents were prepared, signed by all partners and forwarded to EC in October 2013. The official start of ADDAPT was November 1, 2013. The Grant Agreement (GA) was signed by the coordinator, TUD, on November 7, 2013 and by the EC on November 14, 2013. With delay the GA forms A were completely signed by all project partners in January 2014. In parallel the Consortium Agreement (CA) was prepared by TUD and discussed with the partners. The final CA was issued on January 7, 2014 and afterwards signed by all partners. The duly signed CA was forwarded to the ADDAPT partners by February 4, 2014.

On the basis of the signed GA and CA the distribution of the project pre-financing for the first project phase was prepared by the coordinator. According to the percentage on the overall project cost/funding of the corresponding partner, the pre-financing shares were transferred to the partners by January 24, 2014. As requested by the EC the project partner PTL received at first only the half of their pre-financing. With progress of the project, the second part of the pre-financing for PTL was transferred by May 14, 2014.

Consortium status

As stated in the DoW and in the GPF documents the ADDAPT consortium consists of 8 partners from 7 European countries. No changes within the consortium have been applied. In Table 14 the current status of the consortium is summarized.

Table 14: ADDAPT consortium status

No.	Name (short)	Country	Contact Persons
1	Technische Universität Dresden (TUD)	Germany	Coordinator: Frank Ellinger Operational Manager: Ronny Henker Administrative: Claudia Hawke
2	IBM Research GmbH (IBM)	Switzerland	Scientific/technical: Thomas Toifl Administrative: Catherine Trachsel
3	VI Systems GmbH (VIS)	Germany	Scientific/technical: Joerg Kropp Administrative: Ljudmila von Berg
4	Argotech a.s. (AT)	Czech Republic	Scientific/technical: Martin Zoldak Administrative: Michal Svoboda
5	Warsaw University of Technology (WUT)	Poland	Scientific/technical: Jaroslaw Turkiewicz Administrative: Elżbieta Tarwacka
6	Compound Semiconductor Technologies (CSTG)	United Kingdom	Scientific/technical: Wyn Meredith Administrative: Mary Kane
7	PrimeTel PLC (PTL)	Cyprus	Scientific/technical: Michael Georgiades Administrative: Dora Christofi
8	Tyco Electronics Nederland BV (TE)	Netherlands	Scientific/technical: Jeroen Duis Administrative: Karin Verbakel

Concerning the Coordination Team the project coordinator (Frank Ellinger) is supported by the project assistant (operational manger: Ronny Henker) and by the European Project Center of TUD which is responsible for administrative, legal and financial aspects in this project (Claudia

Hawke). Exploitation Manager for ADDAPT is Jeroen Duis (TE). The leaders of the several workpackages (WP) are listed in Table 15.

Table 15: List of WPs and their leaders

WP No.	Name	Leader	Partner
WP1	Management	Frank Ellinger	TUD
WP2	Market studies, exploitation and dissemination, standardization	Jeroen Duis	TE
WP3	Network analysis, system design and verification platform	Thomas Toifl	IBM
WP4	Adaptive optical components	Nikolay Ledentsov	VIS
WP5	Adaptive integrated circuits	Ronny Henker	TUD
WP6	PCB and packaging	Martin Zoldak	AT

Communication between project partners

With the project progress a couple of different ways for the communication among the project partners have been established in ADDAPT. These consist of regular face-to-face meetings or workshops, web-/telephone-conferences, individual phone calls and email correspondence, personnel exchange and data sharepoint.

- Meetings and Workshops:
  Project face-to-face meetings or ADDAPT consortium workshops are planned for approximately every six months. The first project meeting was the kick-off meeting on January 16, 2014 hosted at TUD in Dresden, Germany. During this meeting all the partners and the project itself were introduced in general. The project objectives, tasks and interdependencies were discussed and clarified. First fruitful discussions and decisions opened many aspects for the further work and progress within ADDAPT.
  The second project meeting was held from July 30-31, 2014 at the partner TE in s'Hertogenbosch, Netherlands. During this meeting the project progress of all WPs was presented, updated and open issues were reviewed. One of the main discussions and target of this meeting was to proceed with and find final ideas for the ADDAPT system concept and architecture. The planning of prototype implementations and the full demonstrator was discussed. Furthermore, risk management mainly on technical aspects was initially composed.
  Further project meetings are proposed as follows:
  - December 2014, Optional meeting in Berlin or Dresden or via webconference
  - ~February 2015, 3rd project meeting @ 1st review meeting, EC, Brussels, Belgium
  - July/August 2015, 4th project meeting @ CSTG, Glasgow, UK
  - December 2015, Optional meeting in Berlin or Dresden or via webconference
  - April 2016, 5th project meeting @ 2nd review meeting, IBM, Zurich, Switzerland
  - October 2016, 6th project meeting @ WUT, Warsaw, Poland
  - March 2017, 7th project meeting @ AT, Trutnov, Czech Republic
  - June 2017, 3rd review meeting @ PTL, Limassol, Cyprus

- Web-/telephone-conferences:
  After the kick-off meeting a weekly all hands webconference was organized and is still performed at a fixed and dedicated time slot. These webconferences in the AdobeConnect system are hosted by TUD every Tuesday, 10-12am CE(S)T. They are used for reporting about updates in the WPs, presentation of project results, general technical discussions, administrative issues etc. Besides the informational character of these calls, proposals and decisions for the further research work are undertaken. The outcomes of the webconferences are summarized in minutes and provided to the partners afterwards by TUD.
  Also in smaller groups and within the WPs webconferences are arranged but on an irregular basis. These are mainly for technical discussion and the adjustments of the tasks of the different partners collaborating in the WP or on connected topics.

- Individual phone calls and email correspondence:
  Actual issues and request are directly discussed and clarified between the respective parties and people via phone or if content has to be shared via email.

- Personnel exchange:
  Personnel exchange is used for direct knowledge exchange in specialized areas at a certain partner, for joint experiments and direct exchange of information. For example two researchers of IBM were visiting IBM for an introduction and training in the IBM 14 nm CMOS technology in June/July 2014. Such a stay is very helpful since the knowledge of many experts on site can be used.

- Data sharepoint:
  A secured and encrypted data sharing system was established, as it is shown in Figure 10. This sharepoint is hosted on an owned server at the project partner TE. It is used to exchange data and information which are relevant for the consortium or on which different people within the consortium have to work on. The data includes documents, presentations, reports and project results for instance.

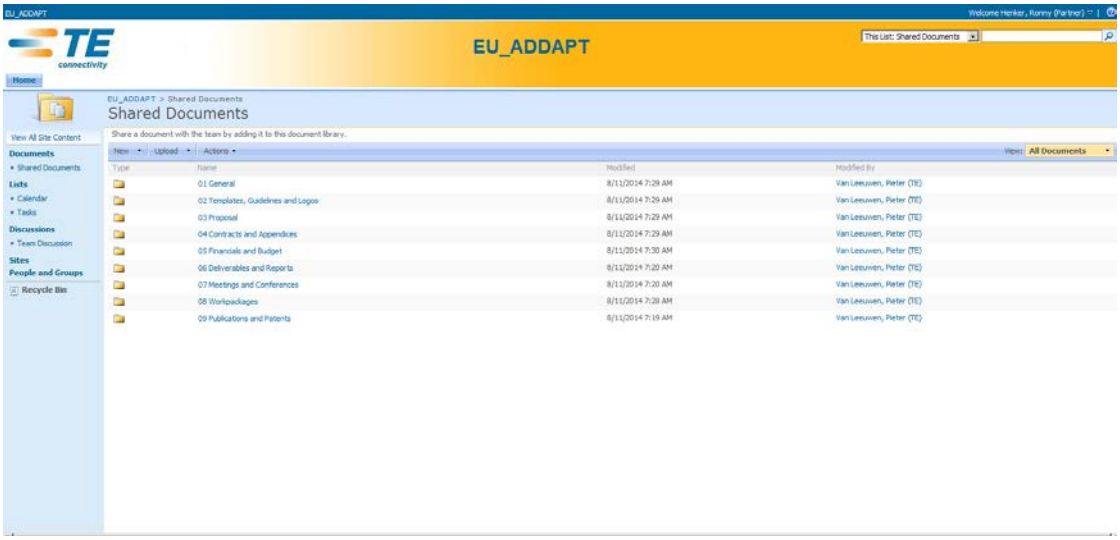
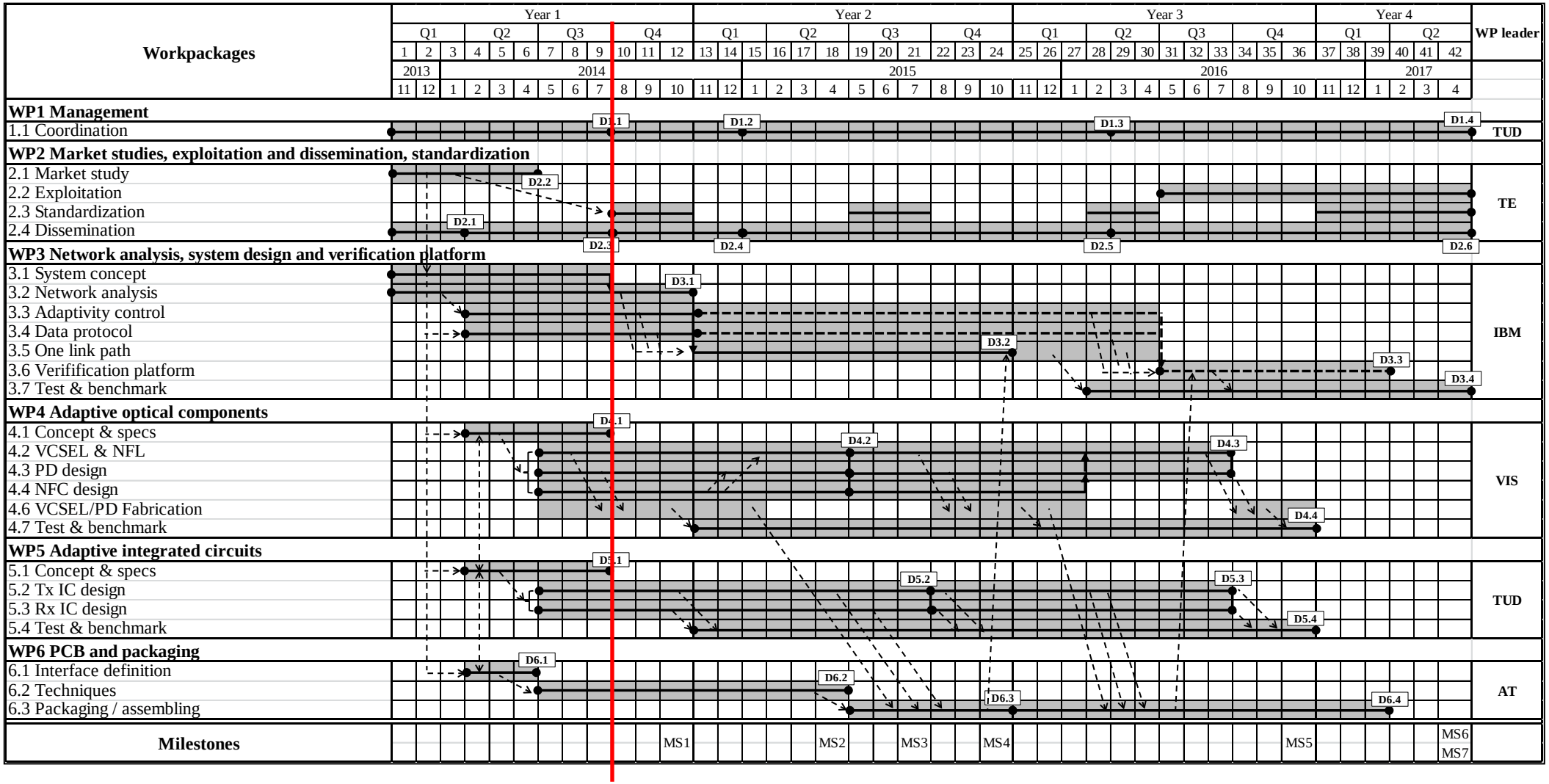


Figure 10: Screenshot ADDAPT data sharing system.

Project planning and status

The work plan of the ADDAPT project is shown in Table 16. This report covers a project period of the first nine months that means until July 2014. Currently all WPs have been started. There are some tasks which are in an advanced state or already finished. This includes for example the market study and interface definitions for the ADDAPT system demonstrator. At the moment the project is in a conceptional and specifications phase where mainly the technical issues and aspects for the components, sub-systems and the final demonstrator are clarified. This includes the concepts and specifications for the system architecture, for the optical devices, for the adaptive ICs and for the packaging and assembling techniques. An intensive network analysis is in progress for several months. Recently, the design phase has been started for the optical devices, the ICs and the packaging techniques. Currently, a detailed manufacturing, assembling and prototyping work plan is elaborated to review and adjust the progress of the device development accordingly. Furthermore, a detailed risk management plan is initiated and in progress to react on different problems during the design and fabrication of the several components. Both, the detailed fabrication and the risk management plan will be reported in the first periodic report.

Table 16: Work plan by means of Gantt chart.



Within the WPs the first deliverables and reports have been prepared and already submitted which are summarized in Table 17. In the following a brief overview of the recent deliverable reports is given:

- D2.1 - Implementation of web-based resource and communication platform
  This deliverable includes the public project presentation, fact sheet and several press releases for instance. Furthermore, the ADDAPT data sharing system as shown in Figure 10 and the project website has been created on the http://www.addapt-fp7.eu/ domain, as it is shown in Figure 11.

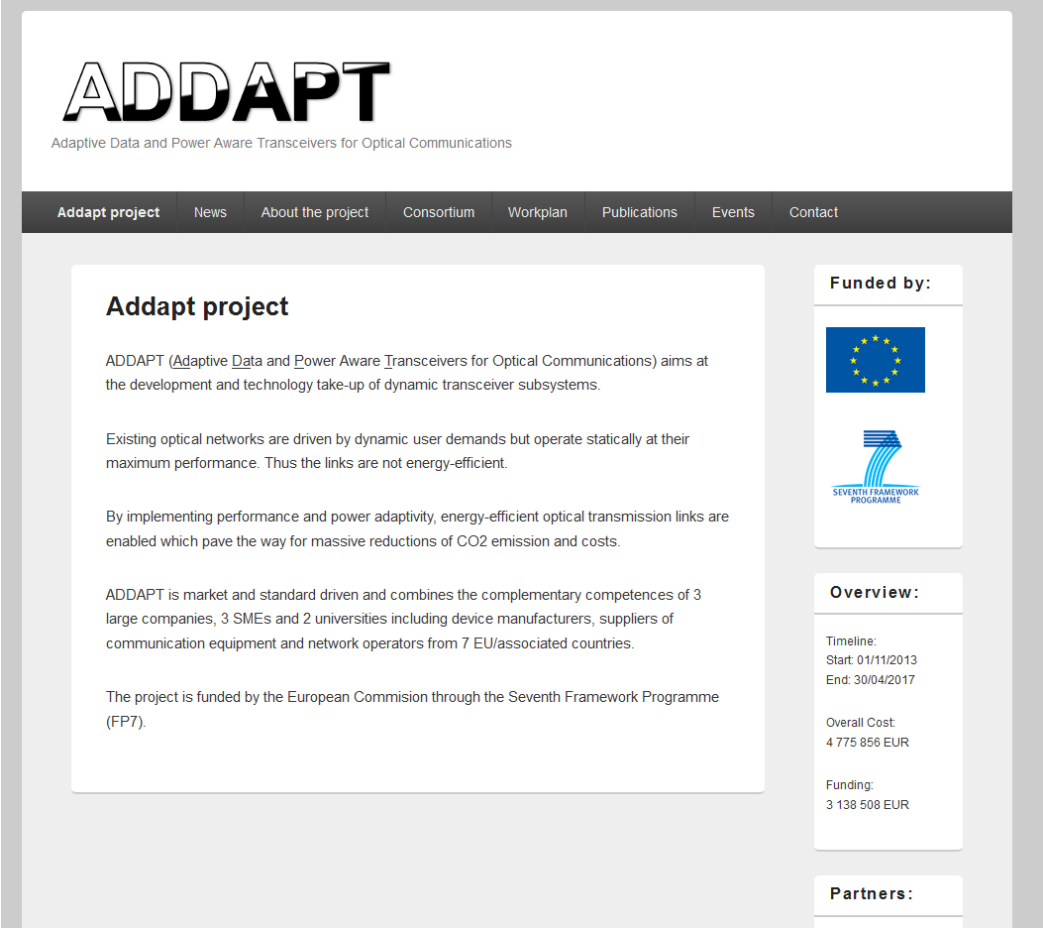


Figure 11: ADDAPT website

- D2.2 - Market study, evaluation of applications and product specifications
  This report gives an overview about existing and foreseen markets, applications and standards in potential fields of ADDAPT. Already existing market surveys from leading suppliers are used to assess market development and the relevance of the ADDAPT technology in those markets. An inventory with respect to the applications is made. Target applications are high-capacity inter-switching (as in data-centers) such as happens between servers, between racks, between co-locations and to storage devices. In supercomputers, the target application is the more direct communication between processors and also to storage devices. Based on those markets, a few first requirements are given for ADDAPT cables. Furthermore, the development of the markets for the relevant protocols are described, and

based on research by Cisco, an estimation of ADDAPT technology cables for the Ethernet domain is made.

- D2.3 - Plans for dissemination and exploitation of results
  This report addresses the first ideas for dissemination ("how the spread the word"), and how to exploit (use the results in the environmental system of the partner's organisation) the findings, this means the know-how and the technologies developed in the framework of this project. Each partner addresses this from his own context and expectations of the project. Therefore, also the market for the ADDAPT technology is briefly recapped from the D2.2 report. Relevant commercial exploitation plans are defined by the project partners in order to obtain an optimal overview of the market potential of the new optical components in electronic and photonic applications. Roadmaps of the new applications will be elaborated and maintained during the project and beyond. More specifically the following activities have been or will be performed in this task: 1) Making an overview of exploitable results expected from the project; 2) Study of the market potential of these exploitable results; 3) Define application roadmaps for these results. In each reporting period this plan will be updated, resulting in the final plan for use and dissemination by the end of the project. This final plan will be presented in D2.6, per April 2017.

- D4.1 - Concepts and specifications for adaptive optical components
  This report is focusing on the concepts of the adaptive optical components which are an important part of the optical cable link. At first, an overview to the assembly concept of the demonstrator for ADDAPT is given which includes the optical coupling of the optical active components of special VCSEL and fast PDs to the waveguides. It is planned to use an optical near field coupling (NFC) of the optical components to the waveguide to achieve an easy coupling situation for the assembly. A design approach and the general concept for the development of fast and near field coupled VCSEL (NFL) is compiled. In addition there is presented the approach for a single mode VCSEL with large emitting diameter as an alternative to reach relaxed coupling conditions. The design concept for high speed PDs and the limitations which must be considered for the NFC are discussed. The technology to manufacture the optical coupling is presented. There will be used polymer optical waveguides for a) the connection of the optical chips on one hand and b) the connection to the standard multimode optical fibers on the other hand.

- D5.1 - Specifications for adaptive transceiver ICs
  This report describes the initial concepts and specifications for the transceiver ICs of the ADDAPT research project. The design includes the main circuits of laserdiode driver (LDD), transimpedance amplifier (TIA), limiting amplifier (LA) and clock- and data-recovery (CDR). These ICs will be designed in 14 nm CMOS technology for high speed with data rates up to 56 Gb/s and lowest power consumption to achieve a high energy efficiency of all together a few pJ/bit. Furthermore, adaptivity with regard to performance (e.g. bandwidth) and power consumption scaling is implemented into the circuits. A rapid switch on/off faster than 20 ns and an adaptive performance tuning for data rates of 56-28-

14-7 Gb/s enable the reduction of the power consumption in the optical link. Preliminary simulations revealed that a 50 % energy saving is possible by reducing the bandwidth by 50-70 %. The design of the circuits already started and a first 14 nm CMOS tape-out is expected at the end of 2014. Optionally, 28 nm CMOS might be used for additional circuits to verify basic circuit and adaptivity approaches.

- D6.1 - Packaging concept and interfaces
  The electrical and optical packaging techniques are key drivers of final product or solution design approaches. There is a specific chain of technologies behind each packaging technique needed for assembly operations. Each packaging technique provides some pros and cons. It is always a question of target product performance, technology chain availability, costs and other side effects like robustness etc. In case of ADDAPT project the electrical packaging will require high-speed performance of electrical lines of 56 Gb/s per each single line in multichannel configuration. The optical packaging will require high-efficiency coupling of high frequency optical signals into multi-mode fiber (MMF) together with investigation of near-field coupling (NFC) technique by minimizing the side effects which can distort the high-frequency (HF) optical signal in MMF solutions. Based on selected packaging technique the component electrical and optical interfaces have to be defined accordingly.

Outlook

In the following project period, further management actions have to be performed and implemented. By the end of 2014 the first project periodic report (deliverable D1.1) has to be presented which includes also the financial statements of each partner. Furthermore, the system concept and network analysis are expected to be finished which will be concluded in the deliverable report D3.1.
Regarding the communication among the partners the weekly webconferences will be reorganized. Since the intensive discussions on the system and demonstrator concepts will be reduced once the system architecture has been completely defined and specified, an all hands meeting might be sufficient once in a month. Therefore, the time slot on the Tuesday can be used for smaller webconferences. In addition, regular calls among the WP leaders and the steering board has to be arranged once there will be no weekly all hands webconference.

3 Deliverables and milestones tables

Deliverables

Table 17: Deliverables

Del. no.	Deliverable name	Version	WP no.	Lead beneficiary	*Nature*	Dissemination level	Delivery date from Annex I (proj month)	Actual / Forecast delivery date Dd/mm/yyyy	Status No submitted/ Submitted	Comments
D2.1	Implementation of web-based resource and communication platform	1	2	TUD	O	PU	M03 (January 2014)	03.02.2014	submitted	Webpage to be updated regularly
D2.2	Market study, evaluation of applications and product specifications	1	2	TE	R	PU	M06 (April 2014)	06.05.2014	Submitted	To be updated due to progress of markets
D6.1	Packaging concept and interfaces	1	6	AT	R	PU	M06 (April 2014)	06.05.2014	Submitted	
D1.1	Interim status report	1	1	TUD	R	PU	M09 (July 2014)	03.09.2014	Submitted	This report
D2.3	Plans for dissemination and exploitation of results	1	2	TE	R	PU	M09 (July 2014)	08.08.2014	Submitted	
D4.1	Concepts and specifications for adaptive optical components	1	4	VIS	R	PU	M09 (July 2014)	13.08.2014	Submitted	
D5.1	Specifications for adaptive transceiver ICs	1	5	TUD	R	PU	M09 (July 2014)	03.09.2014	Submitted	

Milestones

None of the scheduled milestones are achieved yet. The first milestone MS1 ‘Concepts & specifications’ will be reached in project month M12 (October 2014). It includes the implementation of the webpage, the evaluation of applications and markets from point of view of network operator and communications equipment supplier, network analysis, concepts and specifications for transceiver components, and definition of the systems and the packaging.

Table 18: Milestones

Milestone no.	Milestone name	Work package no	Lead beneficiary	Delivery date from Annex I dd/mm/yyyy	Achieved Yes/No	Actual / Forecast achievement date dd/mm/yyyy	Comments

Acronyms

Acronym	Definition
AOC	Active Optical Cable
ASIC	Application-specific integrated circuit
AT	Argotech
BER	Bit error rate
CDR	Clock- and data recovery
CSTG	Compound Semiconductor Technologies Global
DAC	Digital-to-analog converter
DFE	Decision feedback equalization
DoW	Description of Work
DSP	Digital signal processor
FEC	Forward error correction
FEM	Finite element method
FIFO	First in, first out
FPGA	Field-programmable gate array
HF	High frequency
HPC	High performance computing
I/O	Input/output
IC	Integrated circuit
ISI	Inter-symbol interference
LA	Limiting amplifier
LDD	Laserdiode driver
MMF	Multimode fiber
NFC	Near-filed coupling
NFL	Near-field laser
NFPD	Near-field photodiode
NIC	Network Interface Card
PCB	Printed circuits board
PD	Photodiodes
PIN	Positive-intrinsic-negative
PR	Phase rotator
RAS	Reliability, availability, serviceability
RF	Radio frequency
Rx	Receiver
SERDES	Serializer/Deserializer
SME	Small- and medium-sized enterprise
SNMP	Simple Network Management Protocol
TE	Tyco Electronics
TIA	Transimpedance amplifier
TUD	TU Dresden

Acronym	Definition
Tx	Transmitter
VCSEL	Vertical-cavity surface-emitting laser
VIS	VI Systems
WP	Work package
WUT	Warsaw University of Technology

References

[1] J. Proesel, C. Schow and A. Rylyakov, "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-based optical links in 90nm CMOS," in *2012 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, USA, 2012.

[2] T. Benson, A. Akella und D. A. Maltz, „Network traffic characteristics of data centers in the wild,“ in *IMC '10 Proceedings of the 10th ACM SIGCOMM conference on Internet measurement*, New York, USA, 2010.

Appendix

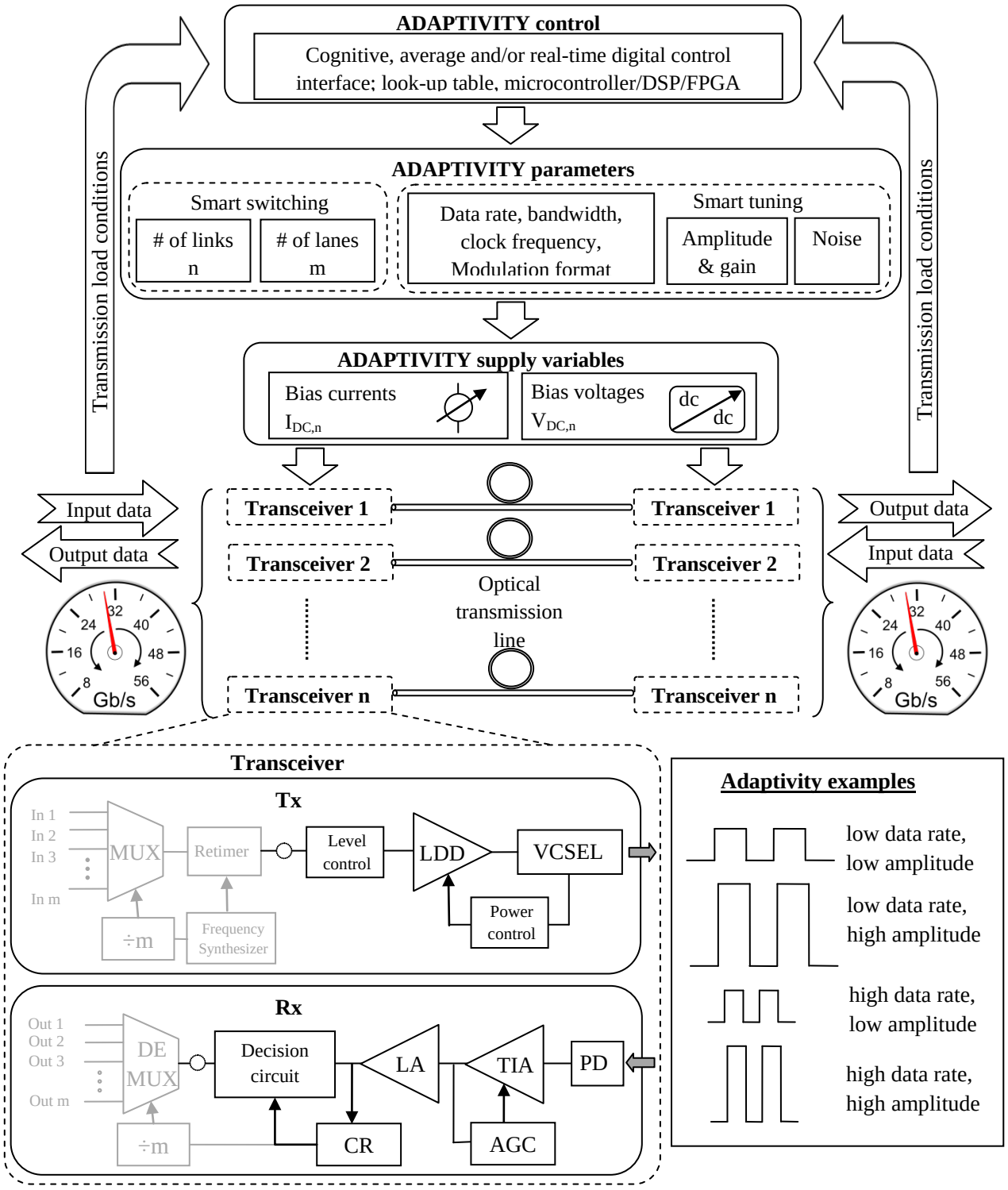


Figure 12: ADDAPT concept

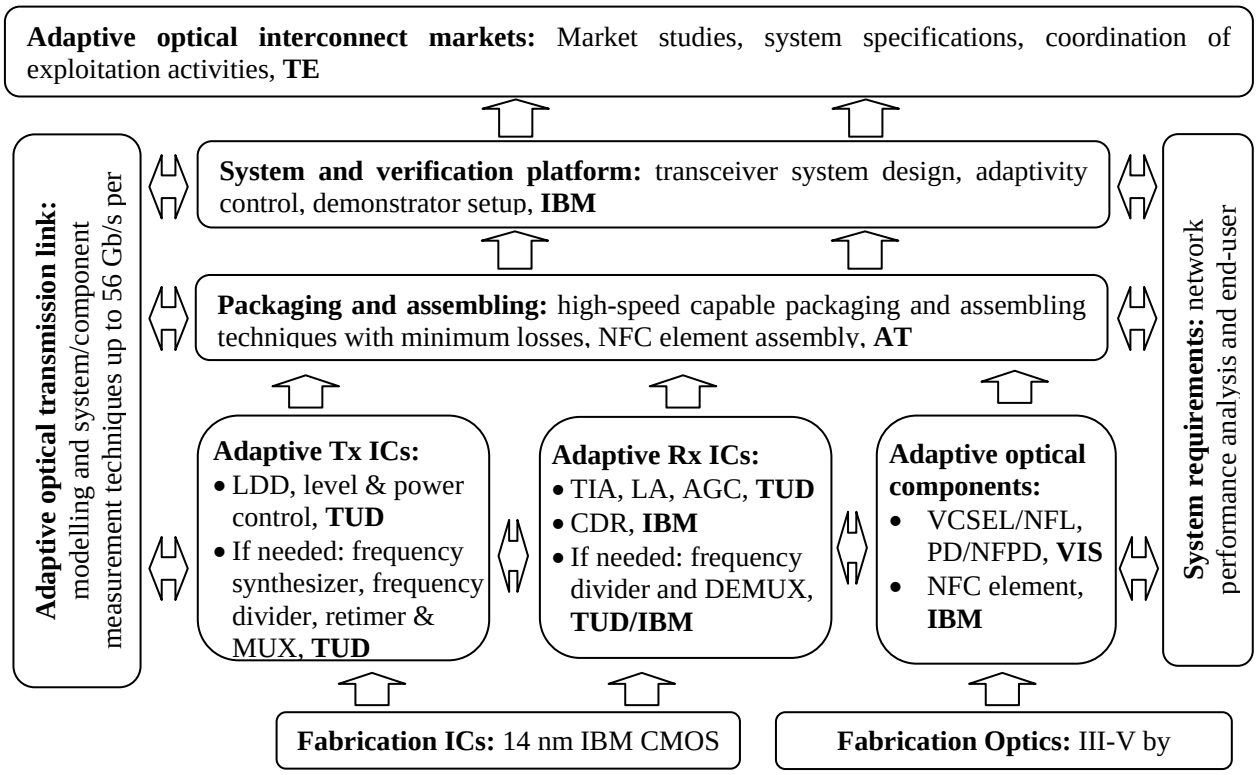


Figure 13: Overview of ADDAPT project structure including key tasks of involved partners