ADDAPT

Adaptive Data and Power Aware Transceivers for Optical Communications

Deliverable Report D 1.3

Project Periodic Report

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Authors	Ronny Henker, Jan Pliva, Mahdi Khafaji, Guido Belfiore, Laszlo Szilagyi, Christina Bogacz (TUD) Thomas Toifl, Alessandro Cevrero, Ilter Oezkaya, Marc Seifried (IBM) Joerg Kropp (VIS) Martin Zoldak (AT) Jarek Turkiewicz (WUT) Iain Eddie (CSTG) Michael Georgiades (PTL) Jeroen Duis, Pieter van Leeuwen (TE)
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Confirmation

Any work or result described in this report is either genuinely a result of this project or properly referenced.

Version Management

Table 1: List of Revisions

Version	Description	Author	Released
V1.0	Document creation, copy of publishable summary, Executive summary	R. Henker (TUD)	April 29, 2016

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Executive Summary

This public deliverable report D1.3 is referred to the Project Periodic Report which has been submitted via Participant Portal and summarizes the progress and financial expenses of the second ADDAPT project phase covering project month M15 (January 2015) to M28 (February 2016). As the project report is confidential due to unpublished and unpatented content, this deliverable report D1.3 is public. It shows the publishable summary of the project report which summarizes the project context and objectives as well as the project progress and results of the first and second project phase.

1 Publishable summary

1.1 *Project context and objectives*

The performance requirements of existing and future optical networks, especially of the optical links and interconnects, are not static and change over time. The individual needs of the users, applications and boundary conditions lead to a strong dynamic behaviour of data rate in today's data networks for instance. However, existing optical networks operate statically at their maximum performance to accommodate the peak traffic requirements and therefore, do not offer much adaptability. Thus, the links are not flexible and not energy-efficient. Therefore, one of the main innovations treated by ADDAPT is to adjust the performance and in turn the power consumption of the multiple optical links from system down to optical device, electrical circuit and transistor level to the actual required data load and link conditions. To achieve this, a high-speed electro-optical transceiver module will be developed whose parameters like bandwidth, modulation format, clock rate, amplitudes can be adapted as it is illustrated in Figure 1. This leads to a reconfiguration of the system according to the actual transmission requirement which in turn reduces the system power consumption. To realize this, a smart adaptivity control is implemented that decides how and when the system parameters need to or may change. The transceiver design includes novel high-speed directly modulated lasers and photodetectors equipped with low-loss low-cost efficient optical coupling, novel adaptive integrated circuits with equalization facilities like laserdiode driver (LDD), transimpedance/variable gain amplifier (TIA / VGA), clock data recoveries (CDR) in advanced 14 nm CMOS technology and high-speed low-loss packaging solutions using glass or ceramic substrates. A transceiver system with 4 link paths each with adaptive data rates from 7 Gb/s up to 56 Gb/s and maximum 10 m link distance is targeted. Further goals are low power consumption and high energy efficiency of the transceiver and its components as well as low latency data transmission. The development of such an adaptive optical interconnect paves the way to build flexible energy-efficient optical transmission links and networks coping with varying bitrate demands and pave the way for massive reductions of CO_2 emission and costs.

Key applications of ADDAPT are optical interconnects for short range data communication, e.g. in data-centers or high performance computing (HPC), for rack-to-rack, server-to-server and board-to-board connections. One possibility would be to replace standard fixed performance and power consumption active optical cables (AOC) with ADDAPTive transceiver.

To achieve the project goals, the ADDAPT consortium involves a full supply chain from semiconductor technologies, component and system design over packaging, assembling and characterization to user requirements, interconnect applications and commercial markets. Complementary competences of 3 large companies, 3 SMEs and 2 universities including device manufacturers, suppliers of communication equipment and network operators are combined. Involved EU and associated countries are the Netherlands, Czech Republic, Poland, United Kingdom, Cyprus, Switzerland and Germany.

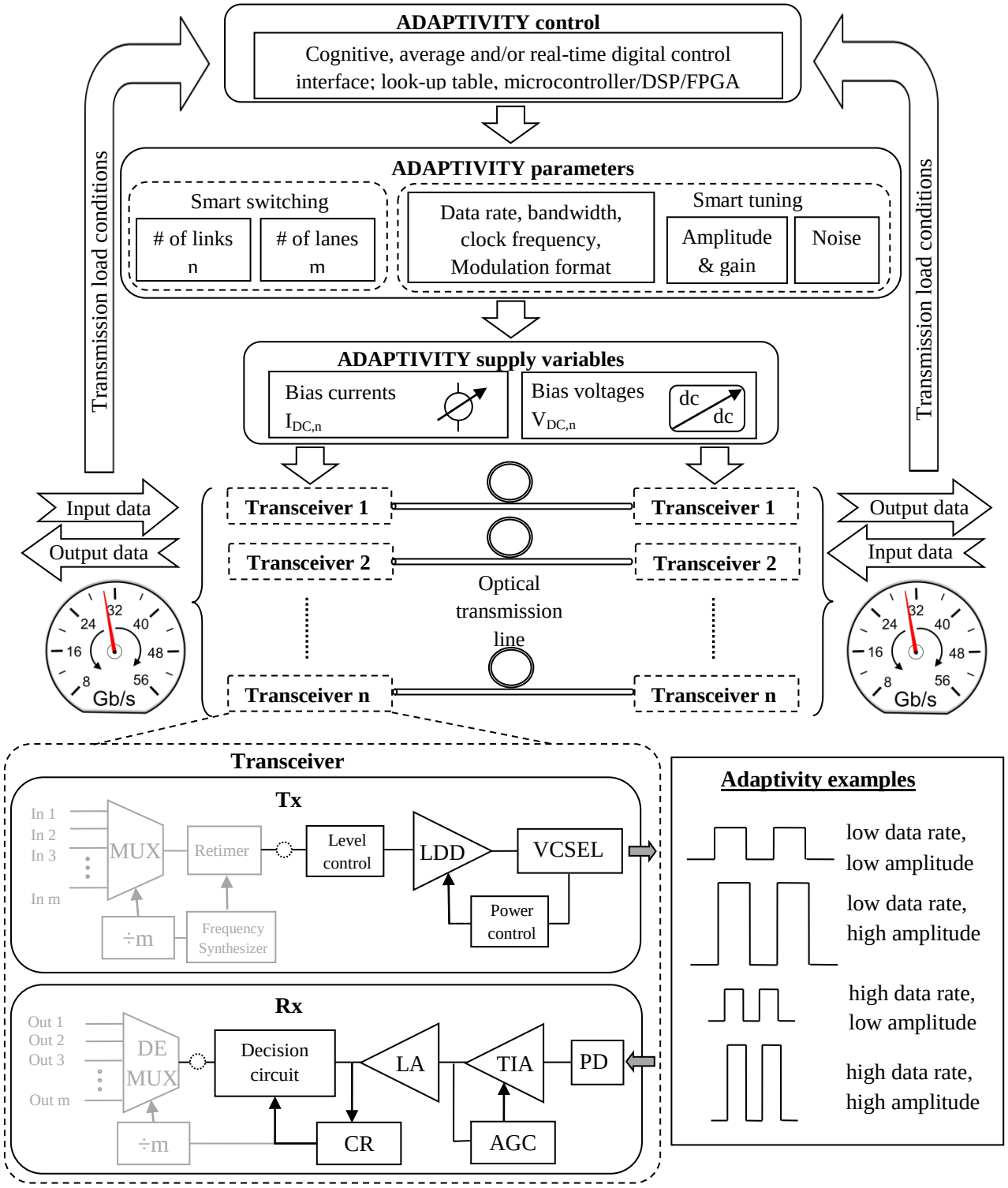

Figure 1: ADDAPT concept.

1.2 *Project progress and results*

Started in November 2013 the project has recently passed the second project period. ADDAPT will be finished by April 2017. In the first project period from November 2013 to December 2014 the project has successfully been launched and elaborated from management point of view. The main research focus was on system and component specifications. Concepts for the high-speed adaptive energy-efficient 4 lane system have been defined and the design of the first components has been started. During the first project period, 10 project deliverables with reports have been provided which state the progress and results.

An intensive market, application and standardization study shows the huge potential of the ADDAPT technology in HPC and data-center environments. Appropriate dissemination and exploitation activities have been defined. A long term network analysis over one year revealed that the link utilization in a data center is on average indeed below 50 % which makes the ADDAPTive techniques reasonable.

A first system concept with 4 link lanes each running up to 56 Gb/s with less than 4 pJ/bit and equipped with adaptive rapid on/off switching (< 20 ns) and smart speed tuning functionality between different data rates (56-28-14-7 Gb/s) for additional power savings was developed. This is based on a master-slave concept with one master lane always running to keep the phase information for a fast wake-up of the slave lanes.

For the optical components including vertical-cavity surface-emitting lasers (VCSEL) and photodiodes (PDs) improved designs and fabrication processes were investigated. However, it turned out that equalization has to be applied by the electrical circuitry to achieve the 56 Gb/s transmission rate. Therefore, big effort was spend in the generation of a reliable VCSEL model. A novel near-field coupling (NFC) concept was developed which enables easy alignment in packaging process.

The initial concepts and specifications for the adaptive transceiver integrated circuits (IC) designed in 14 nm CMOS technology have been derived from the system concept. A high data rate of up to 56 Gb/s and a high overall energy efficiency of maximum <4 pJ/bit is targeted and subject to be optimized for the laserdiode driver (LDD), transimpedance/variable gain amplifier (TIA/VGA) and clock-data-recovery (CDR). Adaptivity in terms of on/off switching and bandwidth/power scaling is implemented into the circuits. To detect the very weak input currents, the receiver (Rx) has to have a high sensitivity and low noise. To provide this a new configuration of low bandwidth TIA, bandwidth compensating DFE and regulating VGA is implemented.

To verify all the concepts and components a packaging concept for a single lane and a 4 lane demonstrator was developed and packaging techniques for 56 Gb/s operation evaluated. The first HF board design iteration including simulations was done. Results show the total insertion loss of demonstrator between ports of IC pad to coaxial connector interface of <3.0 dB. Thermal simulations of the transceiver components revealed that due to the low power consumption the maximum temperature change is just ~ 25 K and therefore thermal inter-component influence is marginal. The design and fabrication of first optical components and ICs as well as packaging test boards were started.

The second project period started in January 2015 and was finalized by February 2016. The main focus of this project phase was on the design, fabrication and verification of the first components.
The system concept was further refined and optimized, as shown in Figure 2. The master-slave concept was overcome and now all lanes can be switched off completely. From the first designs the energy efficiency of the complete single lane link was confirmed to be 4 pJ/bit. The power consumption in different tuning operating modes at 56-28-14-7 Gb/s corresponds to 220-97-58-43 mW which is an 80 % reduction. By further system level simulations which take different network statistics into account, also an up to 80 % power saving at link latencies of 10 % is expected by applying rapid on/off switching to all the four link lanes, as shown in Figure 3.

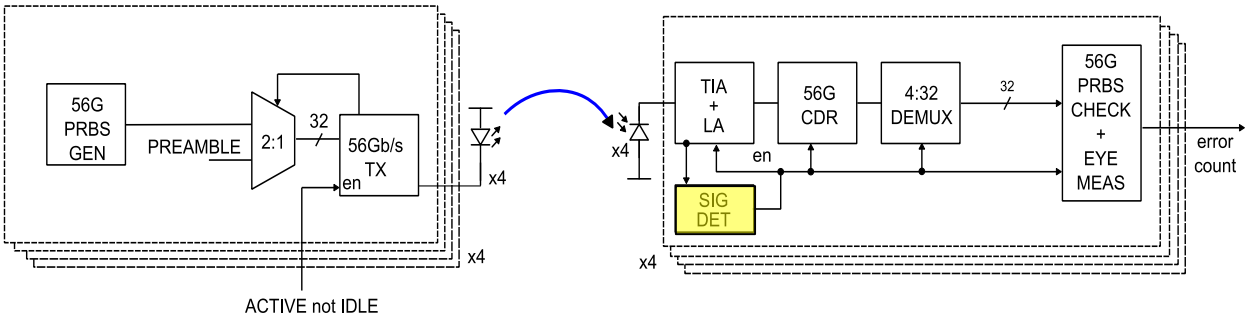

Figure 2: Planned demonstrator with rapid ab-initio CDR with Active/Idle detection.

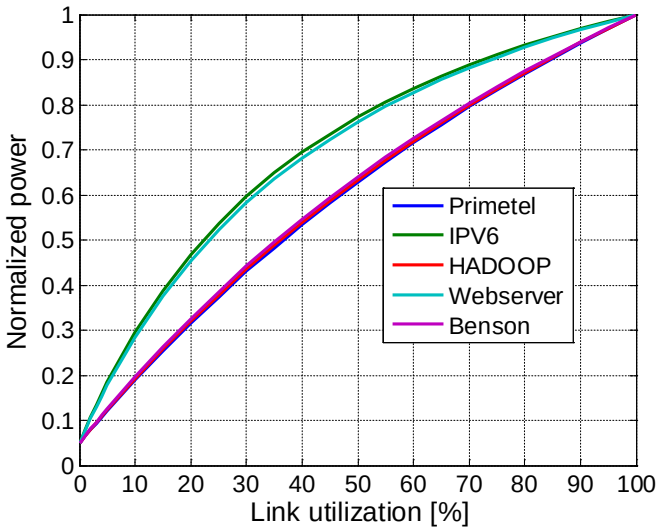

Figure 3: Link power vs. utilization for different packet statistics for switching off all fours lanes.

The first improved VCSEL design was finished and the components were successfully fabricated, as shown in Figure 4. The VCSEL design with small oxide apertures of about 3.5 µm diameters reached single mode emission at reasonable drive currents for the smaller, as shown in Figure 5 (left). First measurements revealed that those devices can operate error-free (BER<10^{-12}) up to 45 Gb/s, as shown in Figure 5 (right). These are currently the fasted VCSELs worldwide. According to the new VCSEL design the laser model has been updated. From studies of the optical NFC approach it turned out that the achievable coupling efficiency will be too low for the application in

ADDAPT demonstrator. For this, a novel scheme based on coupling to a polymer waveguide between the VCSEL and the fiber was developed, while the NFC approach will further be investigated. High-speed PDs have been designed and are in fabrication. Optical transmission experiments with SM-VCSELs and different data formats (NRZ, PAM, MultiCAP) verified the operation of the developed components at high data rates of 50+ Gb/s. These works achieved top publications, e.g. at OCF 2016 post-deadline paper session which only accepts world record results.

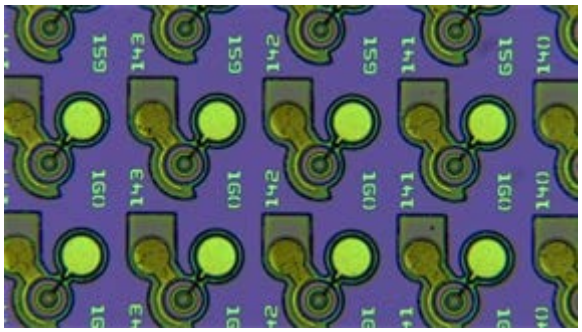

Figure 4: ADDAPT VCSEL-image.

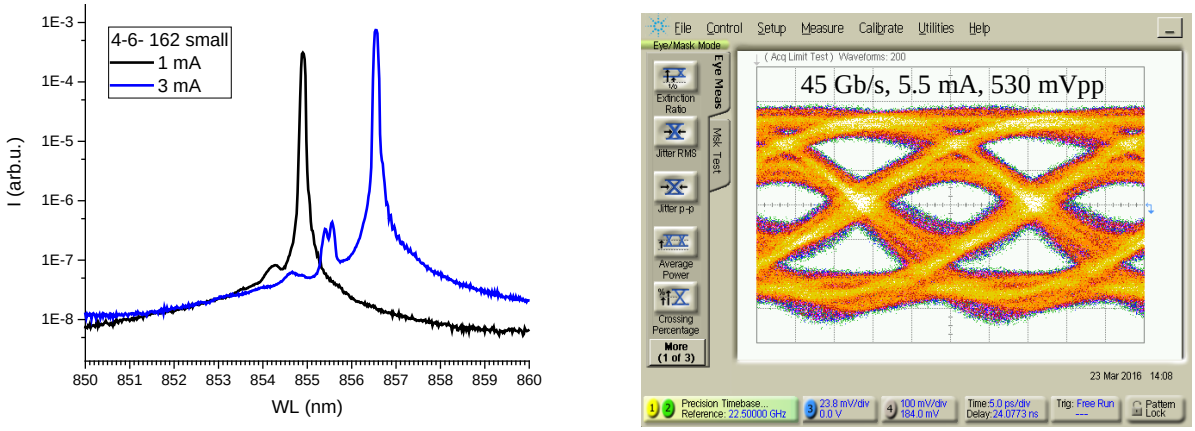

Figure 5: ADDAPT VCSEL. (left) optical emission spectrum; (right) error-free NRZ data modulation at 45 Gb/s.

Also the first IC designs were finished and the first 14 nm chips, including LDD+FFE and Rx AFE with DFE and CDR came back from fabrication. The LDD was successfully measured and show functional FFE and high performance operation at 54 Gb/s, as shown in Figure 6. Several re-designs with rapid on/off functionality and performance adaptivity have been started and taped-out. Currently, an improved version of the Tx LDD and the full Rx system with AFE, DFE and CDR is in fabrication. Additionally, adaptive LDD and TIA circuits have been designed in 28 nm CMOS, fabricated and successfully measured regarding their ADDAPTive potential. By reducing the LDD and TIA performance, power consumption can be reduced by 25 % and 50 %, respectively.

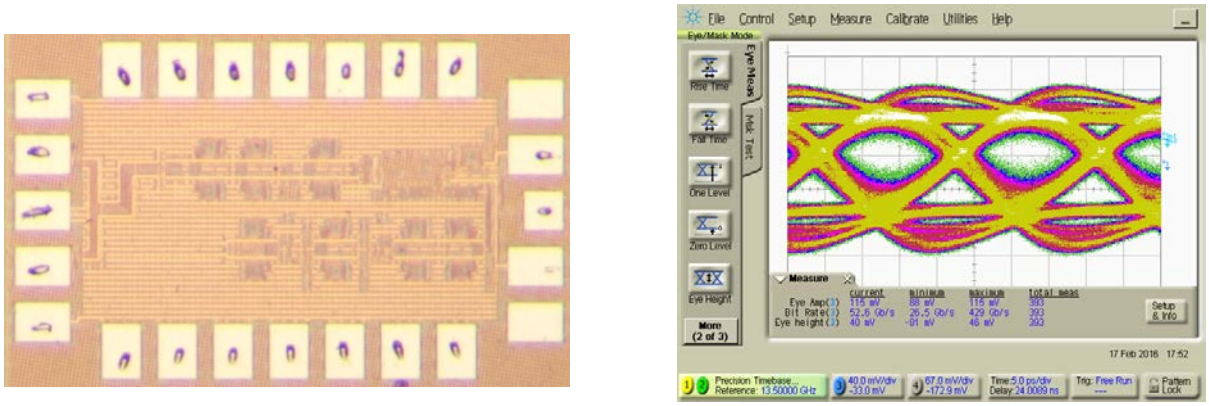

Figure 6: Tx LDD with FFE in 14 nm CMOS; (left) chip micrograph; (right) electrical eye diagram at 54 Gb/s.

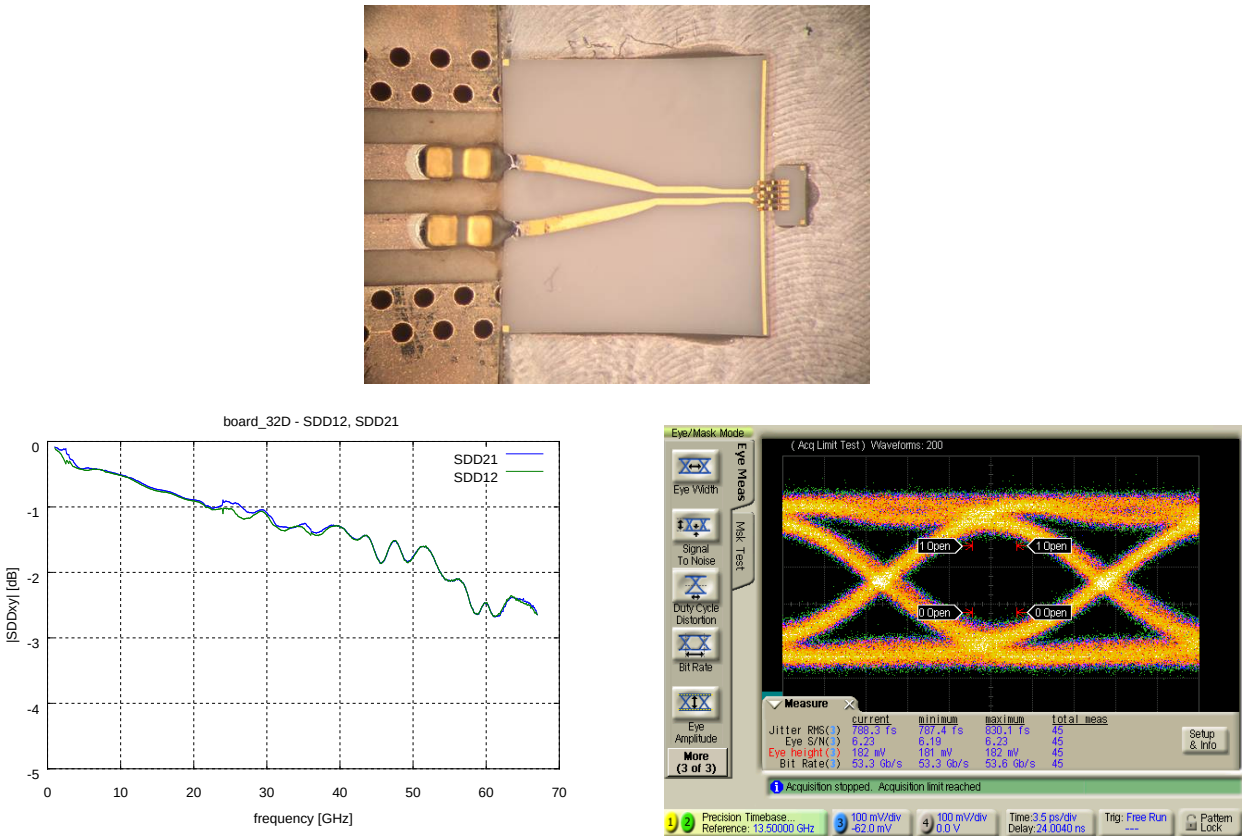

Figure 7: Demo board iteration 2. (top) COAX-GSSG-GSSG configuration; (left) measured S21-parameter; (right) measured eye diagram at 54 Gb/s.

A second iteration of test boards for verification of the used packaging techniques have been designed and fabricated, as shown in Figure 7. Measurements showed that a very low insertion loss of <2 dB up to 50 GHz can be expected for the complete electrical signal path. Large signal measurements confirmed an error free electrical data transmission up to leading edge 54 Gb/s. On the basis of verified packaging techniques and board designs the test boards for the single lane demonstrator have been realized and the link can be packaged now.

Besides the technical progress further management activities guaranteed the successful progress of ADDAPT. Further studies on market potentials and competitive solutions still confirm the high impact of the project in the field of data communication in data center and HPC environments. Finally, further dissemination actions in terms of publications for instance and exploitation plans were performed.

For more details, please refer to:

ADDAPT http://www.addapt-fp7.eu/	Coordination contact at TU Dresden:	
	Prof. Frank Ellinger Tel.: +49 351 463 38734 frank.ellinger@tu-dresden.de	Dr. Ronny Henker Tel.: +49 351 463 33084 ronny.henker@tu-dresden.de

Acronyms

Acronym	Definition
AOC	Active optical cable
CDR	Clock data recovery
HPC	High performance computing
LA	Limiting amplifier
LDD	Laserdiode driver
MBO	Mid-Board-Optics
NFC	Near field coupling
TIA	Transimpedance amplifier
VGA	Variable gain amplifier