ADDAPT

Adaptive Data and Power Aware Transceivers for Optical Communications

Deliverable Report D 6.1

Packaging concept and interface definition

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Executive Summary

The electrical and optical packaging techniques are key drivers of final product or solution design approaches. There is a specific chain of technologies behind each packaging technique needed for assembly operations. Each packaging technique provides some pros and cons. It is always a question of target product performance, technology chain availability, costs and other side effects like robustness etc. In case of ADDAPT project the electrical packaging will require high-speed performance of electrical lines of 56 Gb/s per each single line in multichannel configuration. The optical packaging will require high-efficiency coupling of high frequency optical signals into multi-mode fiber (MMF) together with investigation of near-field coupling (NFC) technique by minimizing the side effects which can distort the high-frequency (HF) optical signal in MMF solutions. Based on selected packaging technique the component electrical and optical interfaces have to be defined accordingly.

1 Introduction

Electronic packaging is a complex and multidisciplinary task which builds together several components to the functional block. It applies both to end products and to components. The wide variety of technologies is related with packaging discipline. There must be taken into account several aspects such as what is a functionality aim, the surrounding interface and the possible ways how it can be achieved. The final packaged component mostly also meets some standards in terms of connection interface, standards in terms of endurance requirements and special criterions required by target industry like telecom, aerospace, defence etc. Finally the package should protect the sensitive components against to electrostatic discharge (ESD).

The goal of ADDAPT project is to demonstrate data transfer for short optical links at very high speeds and at high power efficiency. Such links are required for interconnections in Data Centres and high-performance computing (HPC).

The ADDAPT project combines electrical and optical components which will be co-packaged together. The specialty of project is to achieve 56 Gb/s data bit rate for each single line in multichannel configuration. For example the 4 channel configuration will provide the link speed of 224 Gb/s and with modularity up to 12 channels the 0.675Tb/s can be achieved for instance.

The electro-optical components will be connected via parallel MMF. The optical coupling into MMF should take into consideration two possible approaches. First, optical coupling based on conventional refractive optical element (ROE) and second, based on NFC. The way of optical coupling into MMF has an impact into the final approach of how all the components will be assembled.

The next important driver of packaging approach is high bit rate which each single electrical line shall to meet. The electrical lines have to enable the transfer of the electrical signals with frequencies beyond 40 GHz assuming the data rate of 56 Gb/s and non-return-to-zero (NRZ) signal coding. Designing of such HF electrical lines is based on problematic of electromagnetic field since the 40 GHz signal is becoming to be represented by electromagnetic waves. Therefore, it is a task of 3D modelling and calculation of parasitic capacitances and inductances of each line which are critical for HF signals and must be reduced to minimum. Other way round the parasitic capacitances and inductances influence the impedance of electrical line which should be very close to the target value over the required bandwidth of transferred HF signals otherwise there will occur signal reflection and other effects for non-impedance matching lines which disable transferring of HF signals. Since the multi-channel case has to be considered there is also becoming critical channel to channel crosstalk for HF signals which is exponentially growing with signal frequency. Therefore, also signal crosstalk has to be minimized during design phase otherwise parallel HF signal transfer will not be granted. The complex geometries in terms of electromagnetic field are nowadays solved by numeric simulations based on either deterministic calculations or iterative finite element method (FEM) simulations. Both cases are mostly combined together in terms of HF packaging approach design.

2 Electro-optical packaging

The packaging approach within ADDAPT project has to consider two main points: the optical coupling and HF data transfer both electrical and optical. The aim is to demonstrate that all components including packaging approach are capable to transfer data over multichannel optical link (multiple MMF) with data rate of 56 Gb/s per each channel assuming high power efficiency. The demonstrator which will show this capability will be based on architecture of evaluation boards and will host all active components like integrated circuits (ICs), central processing unit (CPU), optical chips, opto-coupling unit, passives and finally HF electrical connectors providing interface to external systems. The HF electrical connectors are the main driver of demonstrator architecture since they should enable to transfer the signals beyond 40 GHz. There are standardized and available just only the connectors which are based on coaxial connectors structure and guarantee the bandwidth beyond 40 GHz. Since the data rate of 56 Gb/s per each channel is a novel approach there is not standardized yet any pluggable connection for multichannel 56 Gb/s like available for zQSFP+ packages for speeds of 4x14 Gb/s and 4x28 Gb/s.

2.1 *Optical coupling*

There is a relation between optical coupling and HF packaging approach. Since there should be investigated both coupling cases the NFC and conventional coupling via ROE the packaging concept has to enable it.

Optical coupling of HF signals to MMF which are used for short link connections has to avoid critical effects like back reflections, encircled flux (EF) which both leads to distortion of optical HF signal. Finally, the high coupling efficiency (CE) is required for power-efficient system and achieving the reasonable sensitivity of receiver which will have quite small active area diameter in relation to diameter of core of MMF.

2.1.1 Near Field Coupling

The NFC is based on coupling of evanescent beam modes emitted by laser to the waveguide in the near field. Distance between vertical-cavity surface-emitting laser (VCSEL) emitting area and waveguide is in range of several microns only otherwise any beam will not be coupled then. Besides this the main driver of CE will also be the angle under which the evanescent beam modes will be emitted from VCSEL and coupled to the waveguide.

The VCSEL electrical and optical interfaces should consider all mentioned aspects above related to optical coupling and NFC. In terms of electrical connection there are two main assembly approaches based on either face-down or face-up attach.

In case of using the face-down assembly and NFC the waveguide should be a part of target substrate/board, see Figure 1. Taking into consideration the fact that CE of NFC strongly depends on distance between VCSEL and waveguide and the accuracy must be kept within a few microns it is very challenging to control within face-down attach. Flip chip (FC) bonding can be based on

solder bumps, AuSn or stud bumps where it is quite challenging to control their height during processing.

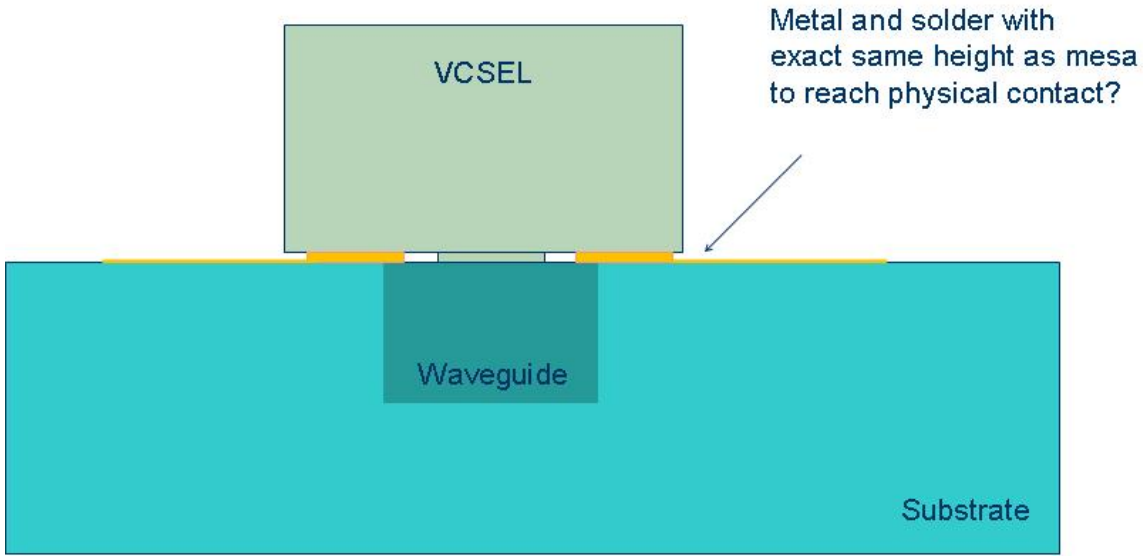

Figure 1: Near-field coupling and flip chip

On the other hand, the face-up attach approach can solve the issue of high accuracy positioning of the waveguide above the VCSEL. But the VCSEL layout of optical and electrical interface has to enable it by avoiding the physical contact between wires and waveguide. Therefore, there should be proper distance between electrical and optical interface in order to enable ideally apply wedge-wedge wire bonding (WB). The VCSEL layout which reflects this requirement is shown in Figure 2.

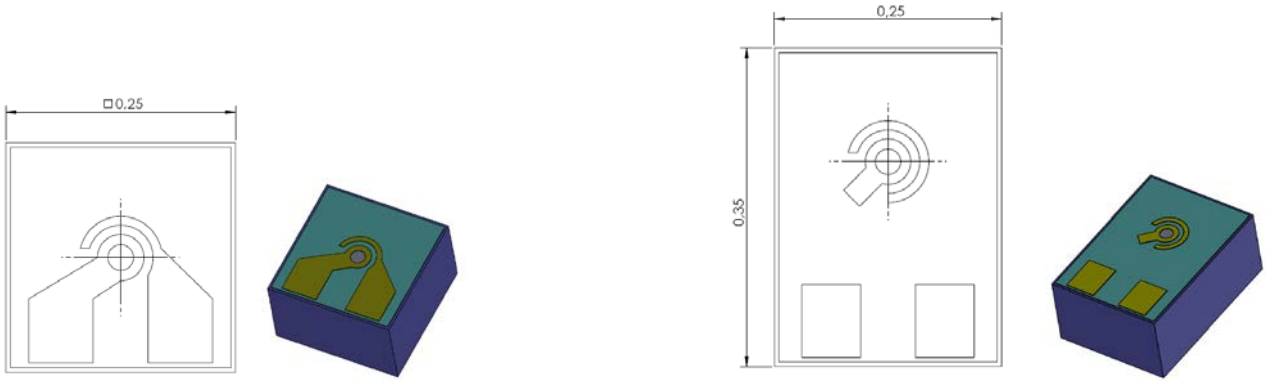

Figure 2: VCSEL interface layout. Left: conventional layout, right: configuration for WB and NFC.

2.2 *Electrical packaging*

Electrical packaging of electronic components is mostly based to two general techniques by face-up or face-down component attach.

2.2.1 Face-down attach

Face-down component attach is represented by FC process where the connections to component interfaces are already solved e.g. via bumps etc. Also in case of opto-electronic chip packaging the optical interface should be a part of the target substrate. The face down attach approach has essential advantages of component interface connection to target substrate in terms HF performance and the packaging process could become more effective in case of high volumes especially for wafer level packaging (WLP). There are also some limitations and disadvantages of face-down attach like less positioning accuracy related to the same costs of face-up attach, high initial costs for small product series and also it could limit some packaging approaches of optoelectronic components as we mentioned in relation with NFC.

2.2.2 Face-up attach

Face-up component attach is a technique where most of the component's interfaces are located upwards from substrate and not toward to substrate. Then there it is necessary to do an interconnection between the component and the target substrate electrical interfaces which is mostly based on WB technique. WB technique has lower HF performance capability compared to FC but based on Argotech's assembly experience it is feasible up to 40 Gb/s per single line. Based on research of Fraunhofer HHI the proper application of WB technique can lead to applications up to 100 Gb/s per single line [1].

Face-up attach approach is used in most of opto-electronic component's packaging since it provides more flexibility to optical coupling in terms of sufficient number of degrees of freedom (DOF) for tolerances compensation, especially for SMF applications. On the other hand the face-down approach has also been becoming to be used for opto-electronic component's packaging especially to MMF applications e.g. Fibre-Lyte by Conjuct Ltd. or Coolbit by TE Corporation.

2.2.3 Demonstrator concept 4x56 Gb/s

Summarising all the aspects mentioned above the demonstrator can be designed as shown in Figure 3 and Figure 4.

There will be the optical chips, ICs and other supporting chips, CPU, HF electrical connectors and coupling element with interface to MTP/MPO conncetors on hosting demonstrator board. The demonstrator is proposed to be done as an hybrid from two basic materials printed circuit board (PCB) and ceramics. PCB will be based on HF laminates as a main hosting board providing high-speed electrical interface. Ceramics will be used for fan out of critical signal lines heading from IC where the critical signal line widths and required accuracies for 40 GHz which on PCB cannot be met at this moment. There are two standardized ceramic materials available for electronic packaging. These are Al_2O_3 and AlN. Both provides similar tgδ factor but different ε_r which has impact in HF design. The tgδ is a dissipation factor which characterizes the losses of dielectric materials and ε_r is a relative permitivity which is a dielectric constant. More critical for HF bandwidth is tgδ and the lower value the better it is. The ε_r have especially an impact in 3D

geometries in terms of impedance matching. Both ceramic materials will be verified during design phase.

The assembly method of components will be primarily based on face-up technique together with WB. The face-down technique is assumed as an alternative solution in case of HF performance issues.

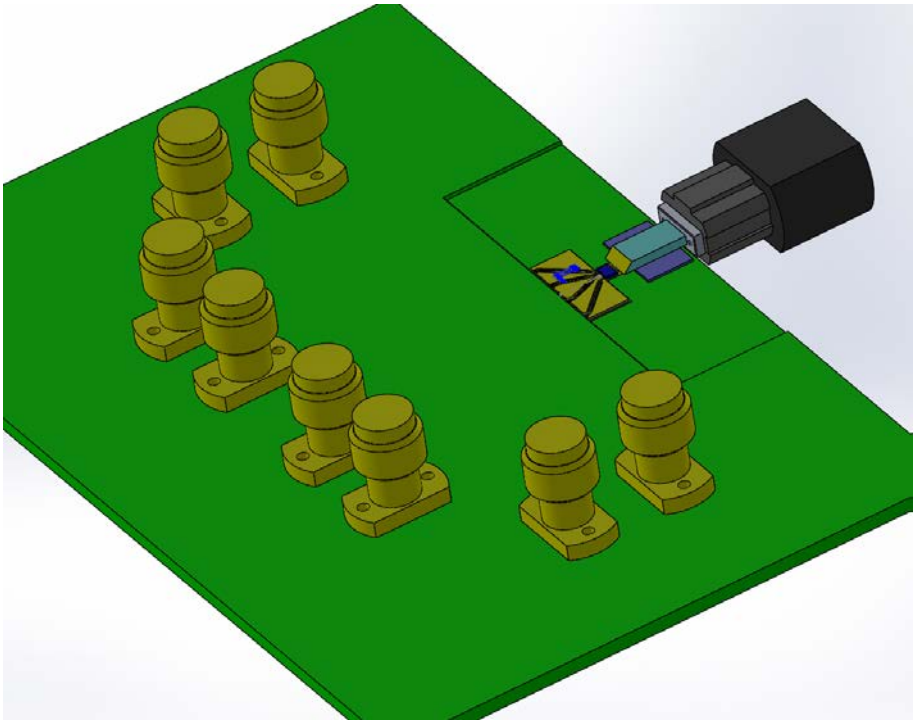

Figure 3: Demonstrator 4x56 Gb/s

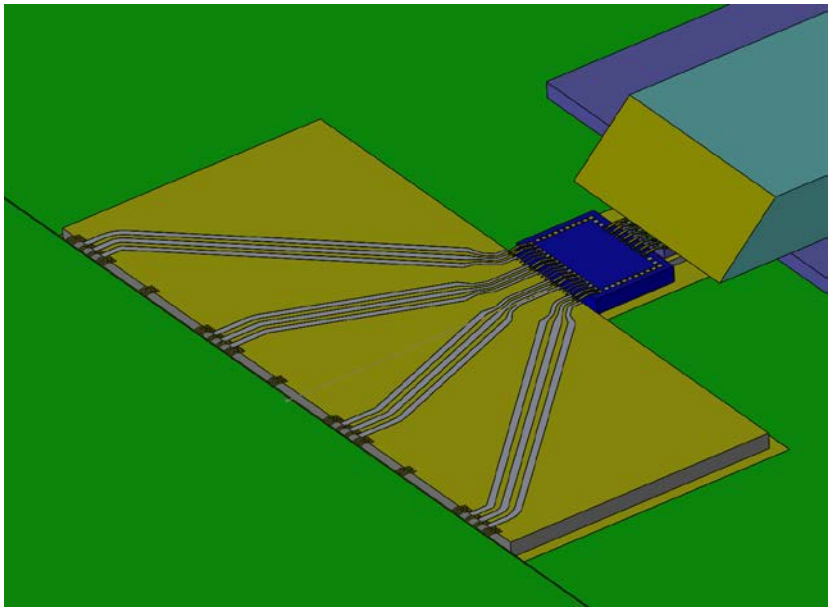

Figure 4: Demonstrator 4x56 Gb/s

The optical coupling will be based on both NFC and conventional ROE. This will enable us to investigate and compare the pros and cons of both approaches in terms of multichannel optical packaging of very high-speed optoelectronic components.

The initial pad layout of IC is shown in Figure 5. This layout has met the requirements for fan out of HF lines up to 50 GHz based on achieved results via simulations, see Figure 6.

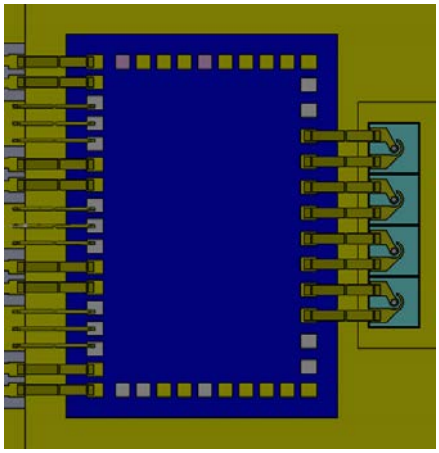

Figure 5: IC layout

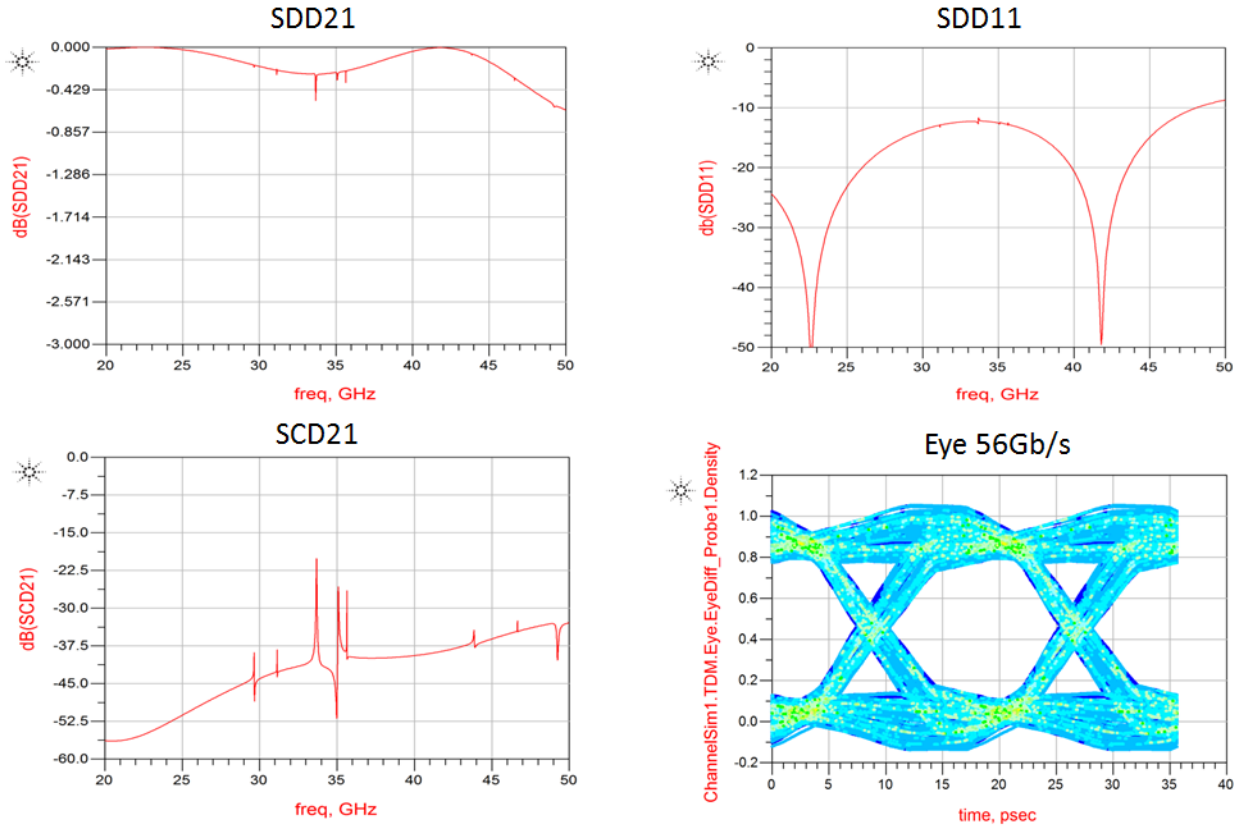

Figure 6: HF simulations of lines fan out on the ceramics

The diagrams in the Figure 6 show the dependency of the differential signal on frequency. Acheived results show very good performance of singal transfer via ceramic board up to 50 GHz. Especially SDD21 shows the attenuation of singal heading to ICs via ceramic board and SDD11 shows the back reflection of input signal connected to ceramic board. Both effects should be minized. The signal attenuation via board should be close to 0 dB and the signal reflected back should have an amplitude as low as possible which represents a good matching to the ceramics board.

3 Conclusion

Packaging approach which has been chosen for ADDAPT project in order to demonstrate the high-speed data transfer rate and power efficient behaviour will be primarily based on face-up technique together with WB. The face-down technique is assumed as an alternative solution. As for optical coupling the near field coupling and conventional ROE coupling will be investigated.

The design phase will investigate several cases of IC pad layouts in relation to ceramic substrate and HF lines fan out. The goal is to minimize the number of grounding pads which could lead to more compact size of IC. There will be also different materials used for boards verified in relation to HF design.

References

[1] Karpuzi Özkan, “Optical and Electrical Co-Packaging – Fraunhofer HHI,” in *Microsys Congress Berlin*, Berlin DE, 2012.

Acronyms

Acronym	Definition
CE	Coupling efficiency
CPU	Central processing unit
DOF	Degree of freedom
EF	Encircled flux
ESD	Electrostatic discharge
FC	Flip chip
FEM	Finite element method
HF	High frequency/very high frequency
IC	Integrated circuit
HPC	High-performance computing/computers
MMF	Multi- mode fiber
NFL	Near-field coupling
NRZ	Non-Return-to-Zero
PCB	Printed circuit board,
ROE	Refractive optical element
SMF	Single-mode fiber
WB	Wire bonding
WLP	Wafer level packaging